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Y540 M/B Schematics Document

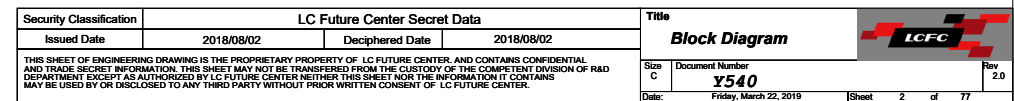
Coffee Lake H-Processor with DDR4 + NV N18E-G1/G0 GPU

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2019-3-22

REV: 2.0

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Cover Page			
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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
15@	15'' Stuff
17@	17'' stuff
7000P@	7000P stuff
7502M@	7502 stuff
8111GUL@	LAN Chip 8111GUL part
8111H@	LAN Chip 8111H part
AG@	Anti-ghost
AOAC@	AOAC support part
BL@	BL
CD@	Cost down part
CNVI@	CNVI support part
DCI@	DCI
Debug@	USB2.0 port 1for Debug
EMC@	EMC part
EMC_8111H@	LAN 8111H EMC Part
EMC_NS@	EMC not-stuff
GC6@	GC6
GYSNC@	GYSNC support part
HDMI@	HDMI
i5@i7@i9@	CPU Part
ME@	ME part(connector, hole)
M6GX6@S6GX6@	VRAM part

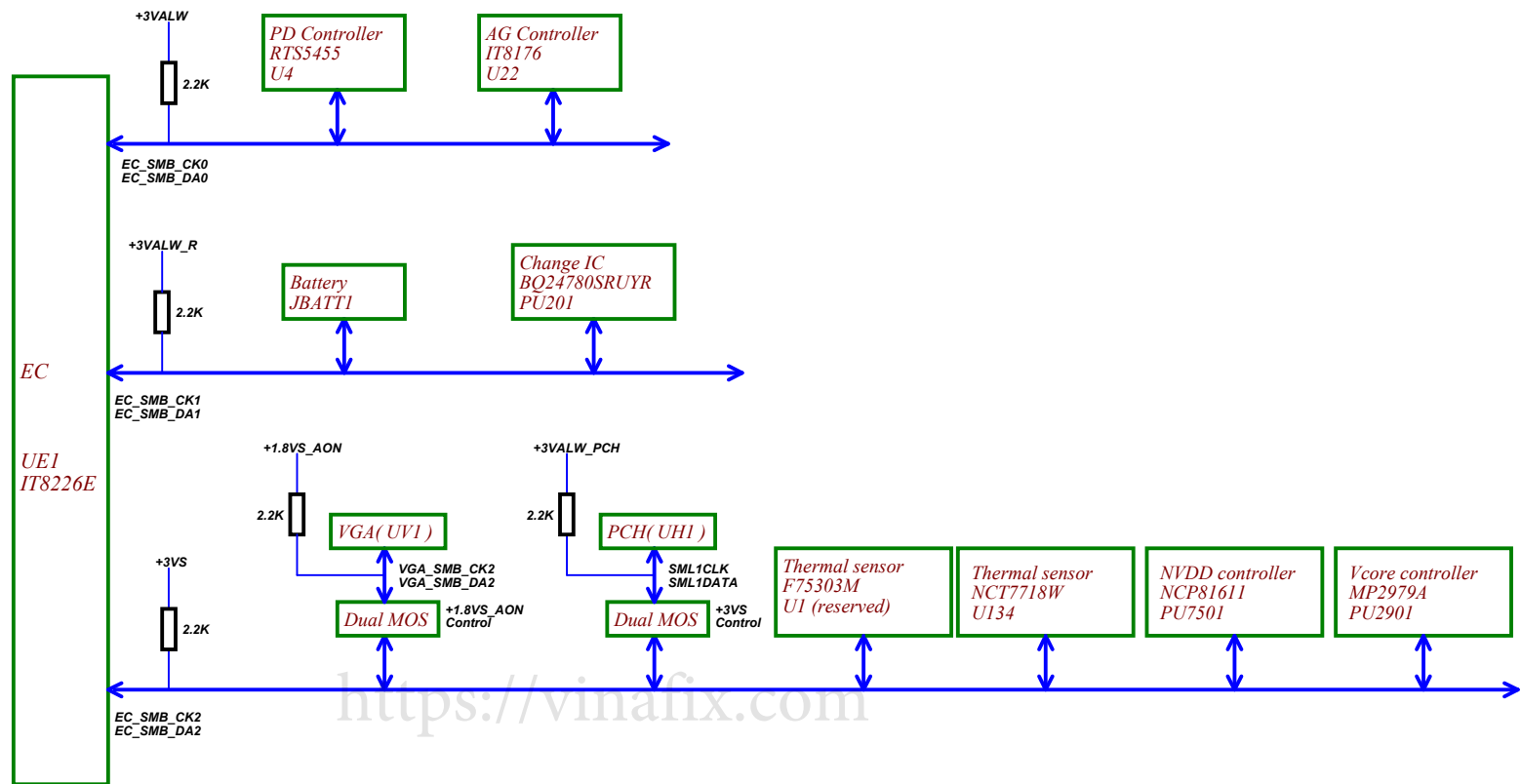
BOM Structure	BTO Item
MIRROR@	MIRROR
N18EG0@N18EG1@	GPU part
NOMIRROR@	17'' stuff
NPI@	SPI VCC diode stuff
OPT@	For NV GPU part
OPTANE@	Optane memory support part
RT8816_NS@	RT8816 not stuff
TPM@	For support TPM sku part
UP1666_@	UP1666 stuff
UP1666_NS@	UP1666 not stuff
UP9632_@	UP9632 part stuff
USB@	USB2.0 port1 for USB Port
X76@	VRAM

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7:8	NA
9	AG
10:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Type-C Port
3	Left USB3.0
4	Right USB3.0
5	NA
6	NA

SATA Port table	
Port	Function
0A	M.2 SSD Gen3
0B	NA
1A	NA
1B	NA
2	NA
3	NA
4	HDD Gen3
5	NA

PCIe Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15:24	NA



SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	HIFI Audio	Anti-ghost
EC_SMB_CLK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	V +3VALW_AG
EC_SMB_CLK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X	X
EC_SMB_CLK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X	X	X	X	X
PCH_SMB_CLK PCH_SMB_DA2	PCH +3VALW_PCH	X	X	X	V +3VS	X	X	X	V +3VS	X	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X	X	X
EC_SMB_CLK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +5VS	X	X

EC SM Bus1 address		EC SM Bus2 address		PCH SM Bus address		PCH I2C 2 Bus address	
Device	Address	Device	Address	Device	Address	Device	Address
Battery	0014	Thermal Sensor F75303M	1001309a b	DDR D180A	1010 000x b	RGB Backlight	
Charger	0001 0010 b	VGA	0a9c (default)	DDR D180B	1010 010x b		
		PCH	Need to update	TP Module	Need to update		
		Thermal Sensor NCT7718W	1001109ab	Wlan	Reserved		

24 PCIE_CRX_GTX_N[0..15]

24 PCIE_CRX_GTX_P[0..15]

PCIE_CTX_C_GRX_N[0..15]

PCIE_CTX_C_GRX_P[0..15]

VCCIO

Note:
Place R_comp inside CPU cavity
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

19 DMI_CRX_PTX_P0 DMI_CRX_PTX_P0 D8 DMI_RXP_0 DMI_TXN_0 B8 DMI_CTX_PRX_P0 DMI_CTX_PRX_P0 19

19 DMI_CRX_PTX_N0 DMI_CRX_PTX_N0 E8 DMI_RXN_0 DMI_TXN_0 A8 DMI_CTX_PRX_N0 DMI_CTX_PRX_N0 19

19 DMI_CRX_PTX_P1 DMI_CRX_PTX_P1 E6 DMI_RXP_1 DMI_TXN_1 C6 DMI_CTX_PRX_P1 DMI_CTX_PRX_P1 19

19 DMI_CRX_PTX_N1 DMI_CRX_PTX_N1 F6 DMI_RXN_1 DMI_TXN_1 B6 DMI_CTX_PRX_N1 DMI_CTX_PRX_N1 19

19 DMI_CRX_PTX_P2 DMI_CRX_PTX_P2 D5 DMI_RXP_2 DMI_TXN_2 B5 DMI_CTX_PRX_P2 DMI_CTX_PRX_P2 19

19 DMI_CRX_PTX_N2 DMI_CRX_PTX_N2 E5 DMI_RXN_2 DMI_TXN_2 A5 DMI_CTX_PRX_N2 DMI_CTX_PRX_N2 19

19 DMI_CRX_PTX_P3 DMI_CRX_PTX_P3 J8 DMI_RXP_3 DMI_TXN_3 D4 DMI_CTX_PRX_P3 DMI_CTX_PRX_P3 19

19 DMI_CRX_PTX_N3 DMI_CRX_PTX_N3 J9 DMI_RXN_3 DMI_TXN_3 B4 DMI_CTX_PRX_N3 DMI_CTX_PRX_N3 19

COFFEE LAKE-H-CPU_BGA1440

@

PCIE_CRX_GTX_P15	E25	PEG_RXP_0	PEG_TXP_0	B25	PCIE_CTX_GRX_P15	OPT@	CC32	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P15
PCIE_CRX_GTX_N15	D25	PEG_RXN_0	PEG_TXN_0	A25	PCIE_CTX_GRX_N15	OPT@	CC16	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N15
PCIE_CRX_GTX_P14	E24	PEG_RXP_1	PEG_TXP_1	B24	PCIE_CTX_GRX_P14	OPT@	CC31	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P14
PCIE_CRX_GTX_N14	F24	PEG_RXN_1	PEG_TXN_1	C24	PCIE_CTX_GRX_N14	OPT@	CC15	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N14
PCIE_CRX_GTX_P13	E23	PEG_RXP_2	PEG_TXP_2	B23	PCIE_CTX_GRX_P13	OPT@	CC30	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P13
PCIE_CRX_GTX_N13	D23	PEG_RXN_2	PEG_TXN_2	A23	PCIE_CTX_GRX_N13	OPT@	CC14	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N13
PCIE_CRX_GTX_P12	E22	PEG_RXP_3	PEG_TXP_3	B22	PCIE_CTX_GRX_P12	OPT@	CC29	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P12
PCIE_CRX_GTX_N12	F22	PEG_RXN_3	PEG_TXN_3	C22	PCIE_CTX_GRX_N12	OPT@	CC13	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N12
PCIE_CRX_GTX_P11	E21	PEG_RXP_4	PEG_TXP_4	B21	PCIE_CTX_GRX_P11	OPT@	CC28	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P11
PCIE_CRX_GTX_N11	D21	PEG_RXN_4	PEG_TXN_4	A21	PCIE_CTX_GRX_N11	OPT@	CC12	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N11
PCIE_CRX_GTX_P10	E20	PEG_RXP_5	PEG_TXP_5	B20	PCIE_CTX_GRX_P10	OPT@	CC27	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P10
PCIE_CRX_GTX_N10	F20	PEG_RXN_5	PEG_TXN_5	C20	PCIE_CTX_GRX_N10	OPT@	CC11	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N10
PCIE_CRX_GTX_P9	E19	PEG_RXP_6	PEG_TXP_6	B19	PCIE_CTX_GRX_P9	OPT@	CC26	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P9
PCIE_CRX_GTX_N9	D19	PEG_RXN_6	PEG_TXN_6	A19	PCIE_CTX_GRX_N9	OPT@	CC10	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N9
PCIE_CRX_GTX_P8	E18	PEG_RXP_7	PEG_TXP_7	B18	PCIE_CTX_GRX_P8	OPT@	CC25	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P8
PCIE_CRX_GTX_N8	F18	PEG_RXN_7	PEG_TXN_7	C18	PCIE_CTX_GRX_N8	OPT@	CC9	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N8
PCIE_CRX_GTX_P7	D17	PEG_RXP_8	PEG_TXP_8	A17	PCIE_CTX_GRX_P7	OPT@	CC24	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P7
PCIE_CRX_GTX_N7	E17	PEG_RXN_8	PEG_TXN_8	B17	PCIE_CTX_GRX_N7	OPT@	CC8	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N7
PCIE_CRX_GTX_P6	F16	PEG_RXP_9	PEG_TXP_9	C16	PCIE_CTX_GRX_P6	OPT@	CC23	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P6
PCIE_CRX_GTX_N6	E16	PEG_RXN_9	PEG_TXN_9	B16	PCIE_CTX_GRX_N6	OPT@	CC7	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N6
PCIE_CRX_GTX_P5	D15	PEG_RXP_10	PEG_TXP_10	A15	PCIE_CTX_GRX_P5	OPT@	CC22	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P5
PCIE_CRX_GTX_N5	E15	PEG_RXN_10	PEG_TXN_10	B15	PCIE_CTX_GRX_N5	OPT@	CC6	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N5
PCIE_CRX_GTX_P4	F14	PEG_RXP_11	PEG_TXP_11	C14	PCIE_CTX_GRX_P4	OPT@	CC21	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P4
PCIE_CRX_GTX_N4	E14	PEG_RXN_11	PEG_TXN_11	B14	PCIE_CTX_GRX_N4	OPT@	CC5	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N4
PCIE_CRX_GTX_P3	D13	PEG_RXP_12	PEG_TXP_12	A13	PCIE_CTX_GRX_P3	OPT@	CC20	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P3
PCIE_CRX_GTX_N3	E13	PEG_RXN_12	PEG_TXN_12	B13	PCIE_CTX_GRX_N3	OPT@	CC4	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N3
PCIE_CRX_GTX_P2	F12	PEG_RXP_13	PEG_TXP_13	C12	PCIE_CTX_GRX_P2	OPT@	CC19	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P2
PCIE_CRX_GTX_N2	E12	PEG_RXN_13	PEG_TXN_13	B12	PCIE_CTX_GRX_N2	OPT@	CC3	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N2
PCIE_CRX_GTX_P1	D11	PEG_RXP_14	PEG_TXP_14	A11	PCIE_CTX_GRX_P1	OPT@	CC18	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P1
PCIE_CRX_GTX_N1	E11	PEG_RXN_14	PEG_TXN_14	B11	PCIE_CTX_GRX_N1	OPT@	CC2	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N1
PCIE_CRX_GTX_P0	F10	PEG_RXP_15	PEG_TXP_15	C10	PCIE_CTX_GRX_P0	OPT@	CC17	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_P0
PCIE_CRX_GTX_N0	E10	PEG_RXN_15	PEG_TXN_15	B10	PCIE_CTX_GRX_N0	OPT@	CC1	1	2	0.22U	0201	6.3V6-K	PCIE_CTX_C_GRX_N0

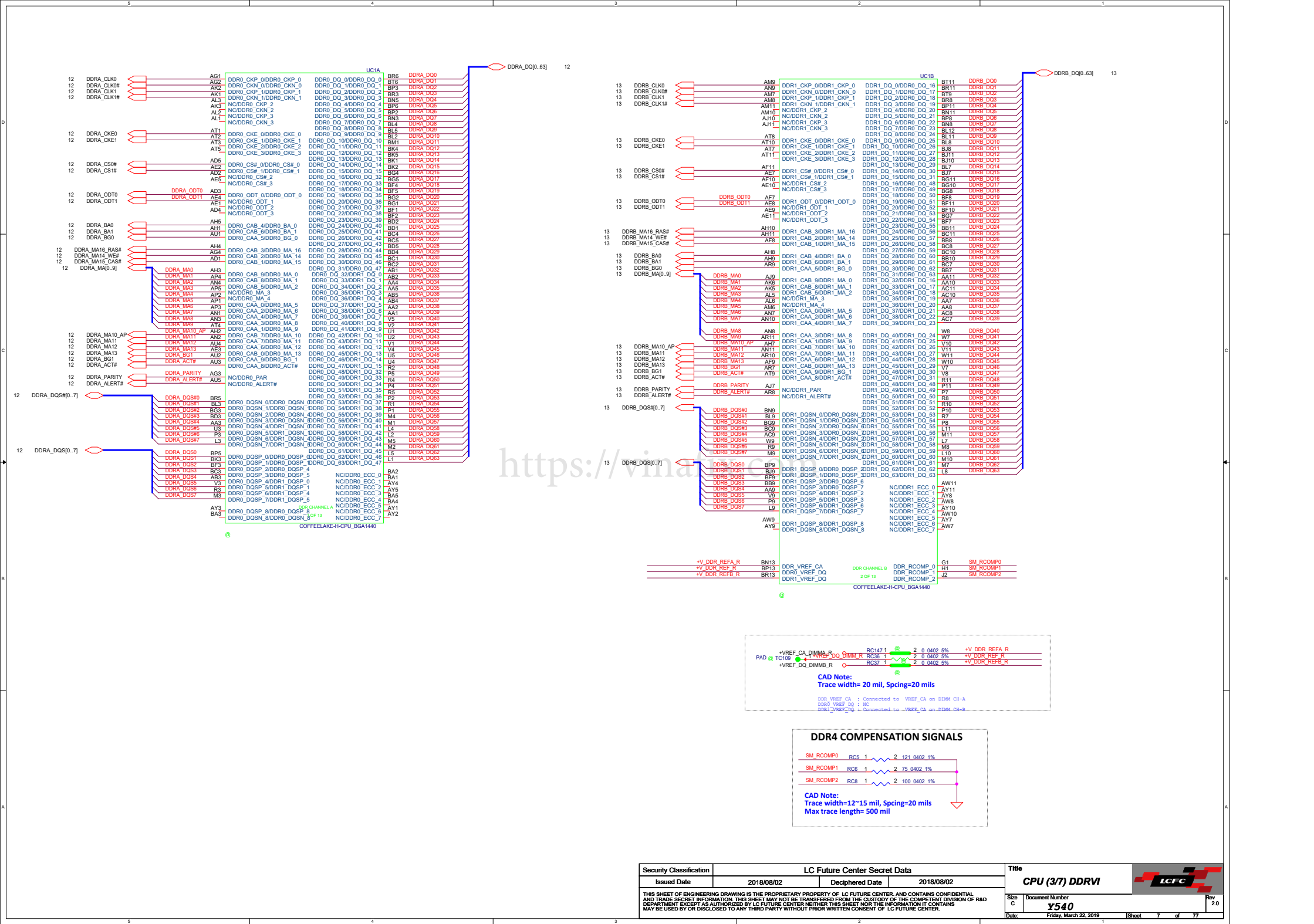
PEG_COMP

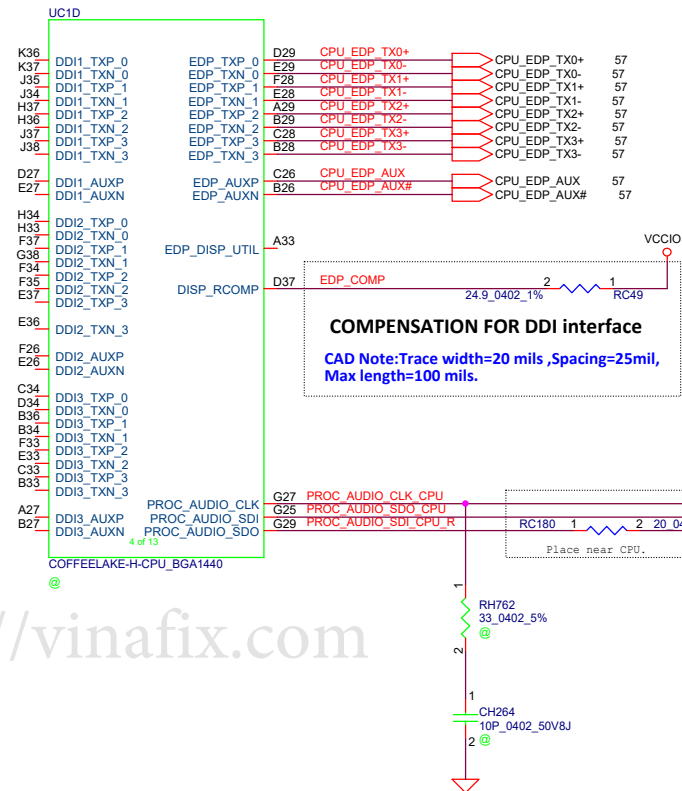
PEG_RCOMP

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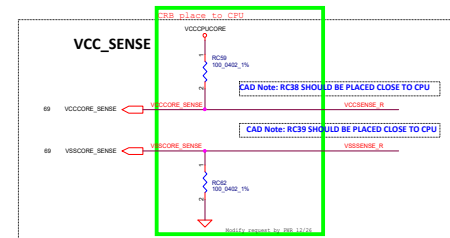
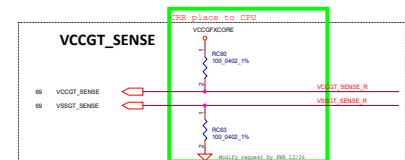
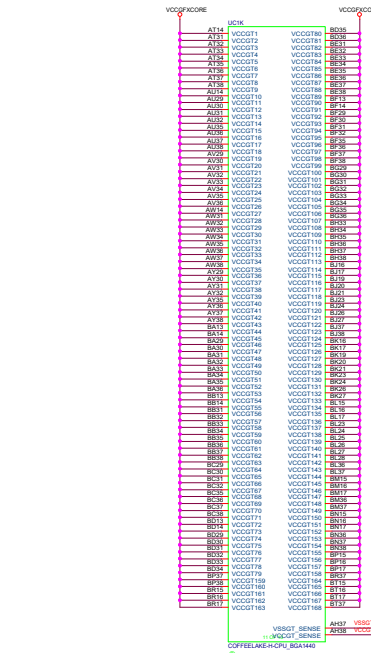
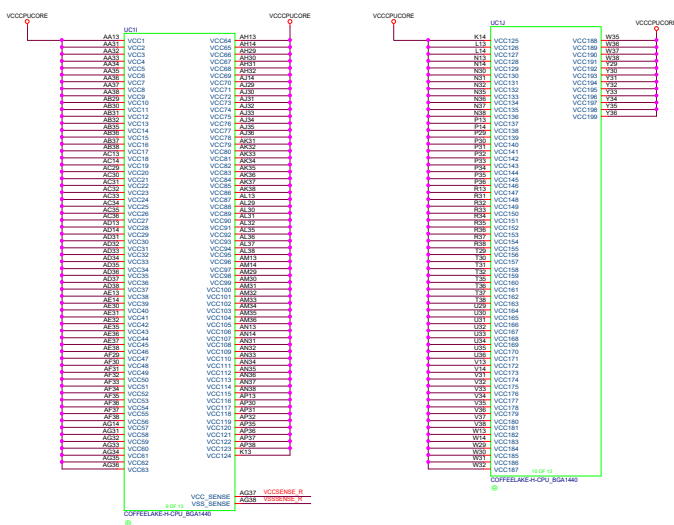
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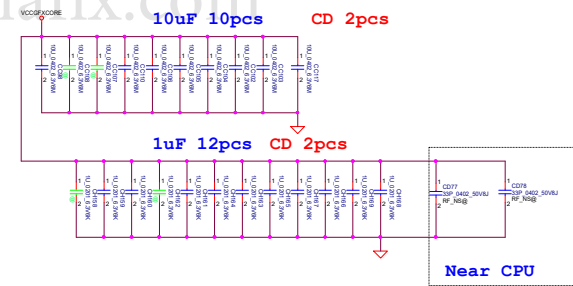
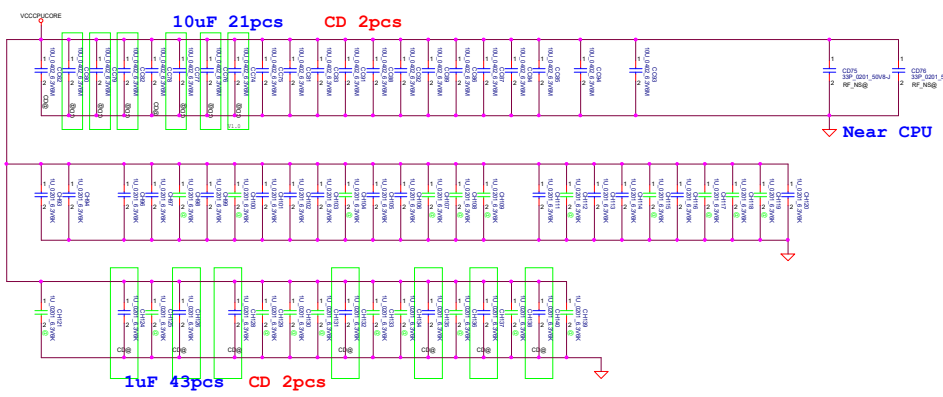
<https://vinafix.com>

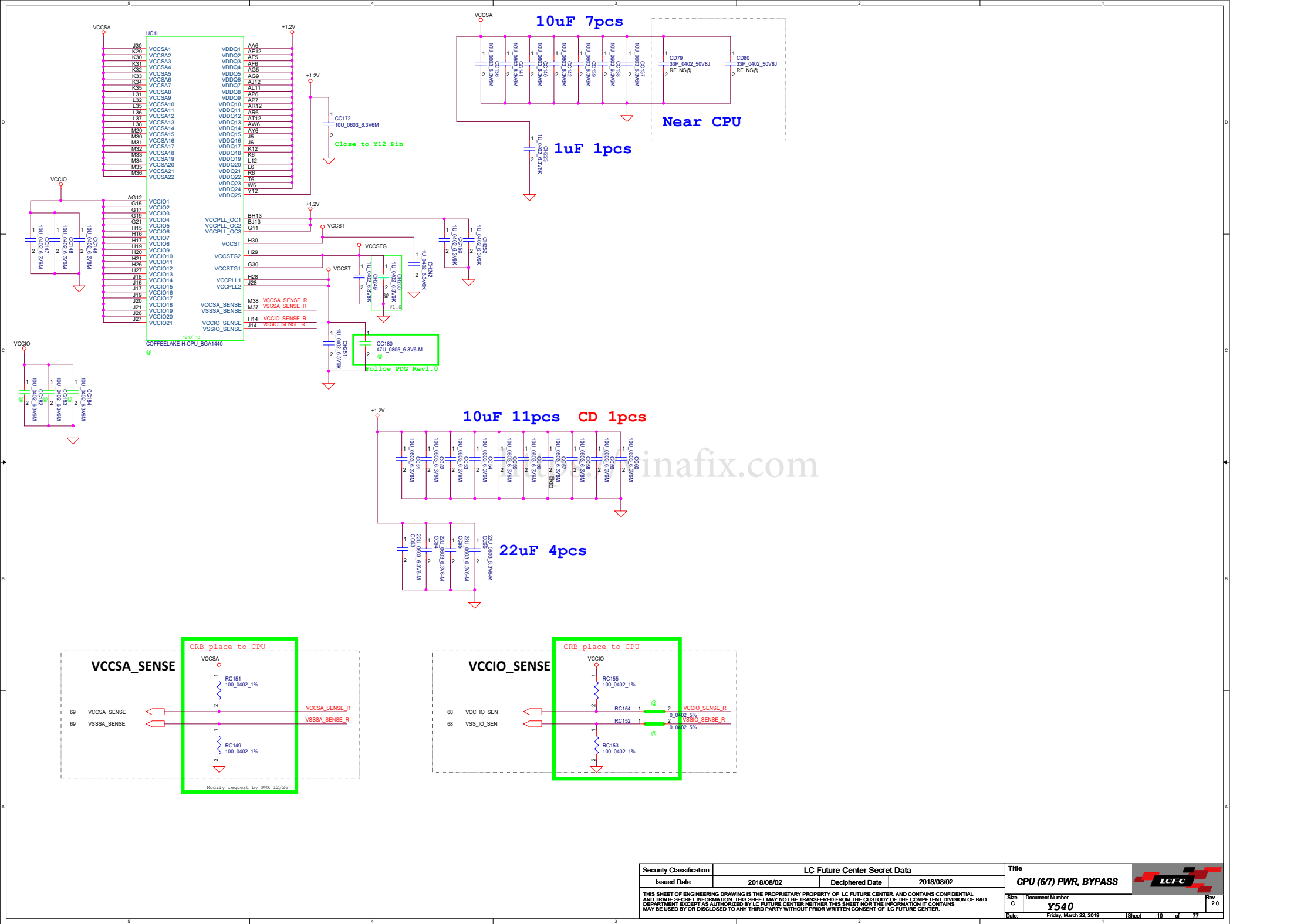
Security Classification		LC Future Center Secret Data				Title CPU (4/7) eDP, DDI			
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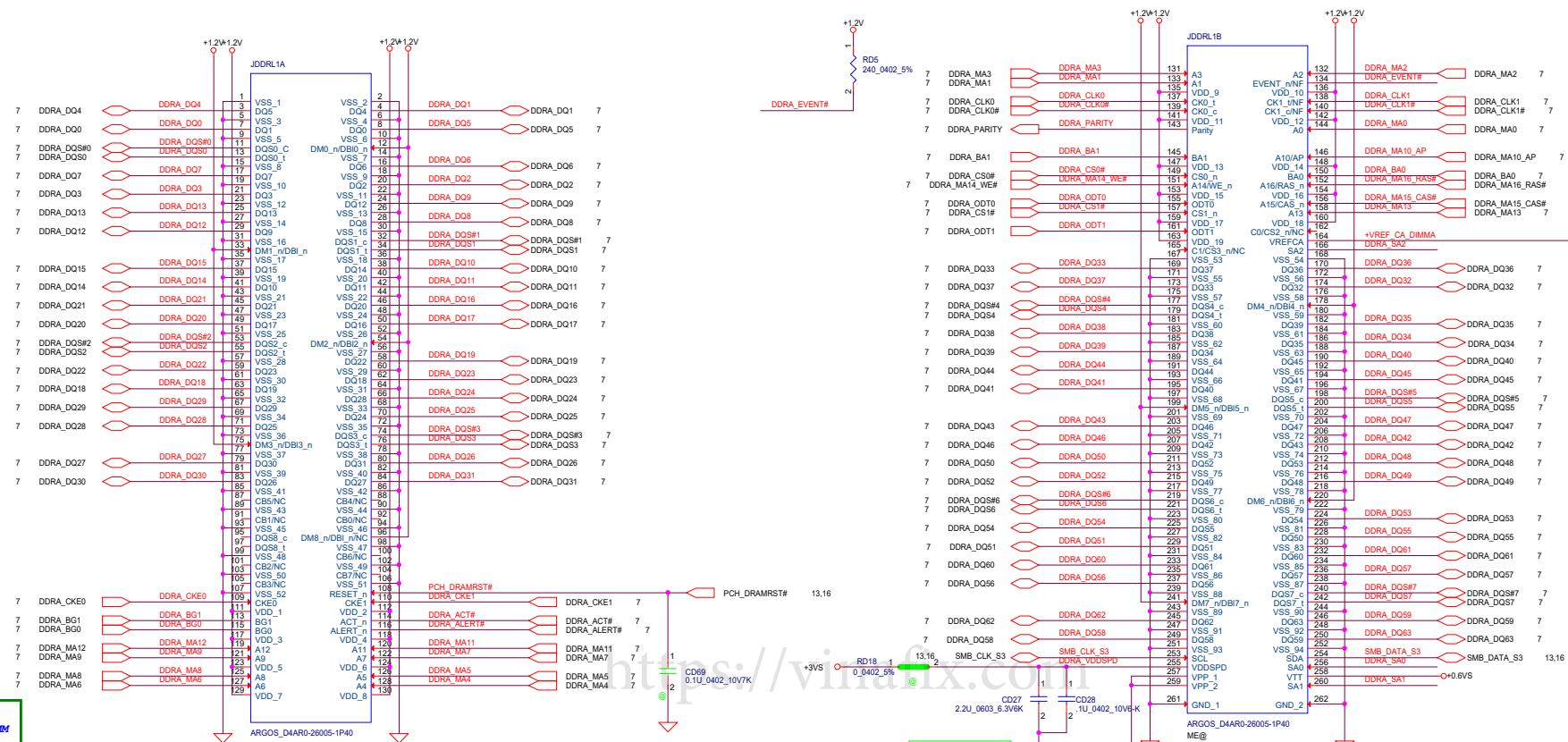
UC1F			
A10	VSS_1	VSS_82	AK4
A12	VSS_2	VSS_83	AL10
A16	VSS_3	VSS_84	AL12
A20	VSS_4	VSS_85	AL33
A22	VSS_5	VSS_86	AL34
A24	VSS_6	VSS_87	AL34
A26	VSS_7	VSS_88	AL7
A28	VSS_8	VSS_89	AL8
A30	VSS_9	VSS_90	AL9
A6	VSS_10	VSS_91	AM1
A8	VSS_11	VSS_92	AM2
AA12	VSS_12	VSS_93	AM12
AA20	VSS_13	VSS_94	AM3
AA30	VSS_14	VSS_95	AM37
AB33	VSS_15	VSS_96	AM38
AB34	VSS_16	VSS_97	AM4
AB6	VSS_17	VSS_98	AM5
AC1	VSS_18	VSS_99	AM12
AC12	VSS_19	VSS_100	AN29
AC2	VSS_20	VSS_101	AN30
AC5	VSS_21	VSS_102	AN5
AC37	VSS_22	VSS_103	AN6
AC38	VSS_23	VSS_104	AP10
AC4	VSS_24	VSS_105	AP11
AC5	VSS_25	VSS_106	AP12
AC6	VSS_26	VSS_107	AP33
AD10	VSS_27	VSS_108	AP34
AD11	VSS_28	VSS_109	AP8
AD12	VSS_29	VSS_110	AP9
AD26	VSS_30	VSS_111	AR1
AD30	VSS_31	VSS_112	AR13
AD6	VSS_32	VSS_113	AR14
AD8	VSS_33	VSS_114	AR2
AD9	VSS_34	VSS_115	AR29
AE31	VSS_35	VSS_116	AR3
AE34	VSS_36	VSS_117	AR30
AED	VSS_37	VSS_118	AR31
AF1	VSS_38	VSS_119	AR32
AF12	VSS_39	VSS_120	AR33
AF13	VSS_40	VSS_121	AR34
AF14	VSS_41	VSS_122	AR35
AF2	VSS_42	VSS_123	AR36
AF3	VSS_43	VSS_124	AR37
AF4	VSS_44	VSS_125	AR38
AG10	VSS_45	VSS_126	AR4
AG11	VSS_46	VSS_127	AR5
AG13	VSS_47	VSS_128	AT29
AG29	VSS_48	VSS_129	AT30
AG30	VSS_49	VSS_130	AT6
AG6	VSS_50	VSS_131	AUT0
AG7	VSS_51	VSS_132	AU11
AG8	VSS_52	VSS_133	AU12
AH12	VSS_53	VSS_134	AU33
AH33	VSS_54	VSS_135	AU34
AH34	VSS_55	VSS_136	AU6
AH35	VSS_56	VSS_137	AU7
AH36	VSS_57	VSS_138	AU8
AHE	VSS_58	VSS_139	AU9
AJ1	VSS_59	VSS_140	AV37
AJ13	VSS_60	VSS_141	AV38
AJ2	VSS_61	VSS_142	AW1
AJ3	VSS_62	VSS_143	AW12
AJ37	VSS_63	VSS_144	AW2
AL38	VSS_64	VSS_145	AW26
AJ4	VSS_65	VSS_146	AW3
AJ5	VSS_66	VSS_147	AW30
AJ6	VSS_67	VSS_148	AW4
W4	VSS_68	VSS_149	W6
W5	VSS_69	VSS_150	V12
Y10	VSS_70	VSS_151	V29
Y11	VSS_71	VSS_152	V30
Y13	VSS_72	VSS_153	AT4
Y14	VSS_73	VSS_154	AD7
Y37	VSS_74	VSS_155	W6
Y38	VSS_75	VSS_156	W7
Y7	VSS_76	VSS_157	W12
Y8	VSS_77	VSS_158	W2
Y9	VSS_78	VSS_159	W3
VSS_79	VSS_79	VSS_160	W33
VSS_80	VSS_80	VSS_161	W34
AK30	VSS_81	VSS_162	W34

COFFEE LAKE-H-CPU_BGA1440

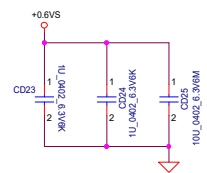
UC1G			
AW5	VSS_163	VSS_244	BJ15
AY12	VSS_164	VSS_245	BJ18
AY33	VSS_165	VSS_246	BJ22
AY4	VSS_166	VSS_247	BJ26
B9	VSS_167	VSS_248	BJ29
BA10	VSS_168	VSS_249	BJ30
BA11	VSS_169	VSS_250	BJ31
BA12	VSS_170	VSS_251	BJ32
BA37	VSS_171	VSS_252	BJ33
BA38	VSS_172	VSS_253	BJ34
BA6	VSS_173	VSS_254	BJ35
BA7	VSS_174	VSS_255	BJ36
BA8	VSS_175	VSS_256	BK13
BA9	VSS_176	VSS_257	BK14
BB1	VSS_177	VSS_258	BK15
BB12	VSS_178	VSS_259	BK18
BB2	VSS_179	VSS_260	BK22
BB29	VSS_180	VSS_261	BK25
BB3	VSS_181	VSS_262	BK6
BB30	VSS_182	VSS_263	BL13
BB4	VSS_183	VSS_264	BL14
BB5	VSS_184	VSS_265	BL18
BB6	VSS_185	VSS_266	BL19
BB12	VSS_186	VSS_267	BL20
BC13	VSS_187	VSS_268	BL21
BC14	VSS_188	VSS_269	BL22
BC33	VSS_189	VSS_270	BL29
BC6	VSS_190	VSS_271	BL33
BD10	VSS_191	VSS_272	BL35
BD11	VSS_192	VSS_273	BL38
BD12	VSS_193	VSS_274	BL6
BD17	VSS_194	VSS_275	BL6
BD14	VSS_195	VSS_276	BM11
BD7	VSS_196	VSS_277	BM12
BD8	VSS_197	VSS_278	BM13
BD9	VSS_198	VSS_279	BM14
BE1	VSS_199	VSS_280	BM2
BE2	VSS_200	VSS_281	BM21
BE29	VSS_201	VSS_282	BM22
BE3	VSS_202	VSS_283	BM23
BE30	VSS_203	VSS_284	BM24
BE4	VSS_204	VSS_285	BM25
BE5	VSS_205	VSS_286	BM26
BE6	VSS_206	VSS_287	BM27
BF12	VSS_207	VSS_288	BM28
BF3	VSS_208	VSS_289	BM29
BF34	VSS_209	VSS_290	BM3
BF6	VSS_210	VSS_291	BM33
BG12	VSS_211	VSS_292	BM35
BG13	VSS_212	VSS_293	BM38
BG14	VSS_213	VSS_294	BM5
BG37	VSS_214	VSS_295	BM6
BG38	VSS_215	VSS_296	BM7
BG5	VSS_216	VSS_297	BM8
BH1	VSS_217	VSS_298	BM9
BH10	VSS_218	VSS_299	BN12
BH11	VSS_219	VSS_300	BN14
BH12	VSS_220	VSS_301	BN18
BH14	VSS_221	VSS_302	BN19
BH2	VSS_222	VSS_303	BN2
BH3	VSS_223	VSS_304	BN20
BH4	VSS_224	VSS_305	BN21
BH5	VSS_225	VSS_306	BN24
BH6	VSS_226	VSS_307	BN29
BH7	VSS_227	VSS_308	BN30
BH8	VSS_228	VSS_309	BN31
BH9	VSS_229	VSS_310	BN34
I2	VSS_230	VSS_311	P38
I3	VSS_231	VSS_312	P6
I33	VSS_232	VSS_313	R12
I34	VSS_233	VSS_314	R29
I4	VSS_234	VSS_315	AT14
I5	VSS_235	VSS_316	BD38
I7	VSS_236	VSS_317	R30
I8	VSS_237	VSS_318	TT
I9	VSS_238	VSS_319	N9
I37	VSS_239	VSS_320	TT1
I38	VSS_240	VSS_321	TT2
I39	VSS_241	VSS_322	TT3
I40	VSS_242	VSS_323	TT4
I41	VSS_243	VSS_324	TT5
I42	VSS_244	VSS_325	TT6

COFFEE LAKE-H-CPU_BGA1440

UC1H			
BN4	VSS_326	VSS_409	F15
BN7	VSS_327	VSS_410	F19
BP12	VSS_328	VSS_411	F2
BP14	VSS_329	VSS_412	F21
BP18	VSS_330	VSS_413	F22
BP21	VSS_331	VSS_414	F23
BP24	VSS_332	VSS_415	F25
BP25	VSS_333	VSS_416	F27
BP26	VSS_334	VSS_417	F29
BP29	VSS_335	VSS_418	F3
BP33	VSS_336	VSS_419	F31
BP34	VSS_337	VSS_420	F36
BP7	VSS_338	VSS_421	F4
BR12	VSS_339	VSS_422	F5
BR14	VSS_340	VSS_423	F8
BR18	VSS_341	VSS_424	F9
BR21	VSS_342	VSS_425	G10
BR24	VSS_343	VSS_426	G12
BR25	VSS_344	VSS_427	G14
BR26	VSS_345	VSS_428	G16
BR29	VSS_346	VSS_429	G18
BR34	VSS_347	VSS_430	G19
BR6	VSS_348	VSS_431	G20
BT12	VSS_349	VSS_432	G24
BT14	VSS_350	VSS_433	G26
BT18	VSS_351	VSS_434	G28
BT21	VSS_352	VSS_435	G4
BT24	VSS_353	VSS_436	G5
BT26	VSS_354	VSS_437	G6
BT29	VSS_355	VSS_438	G8
BT32	VSS_356	VSS_439	G9
BT5	VSS_357	VSS_440	H11
BT11	VSS_358	VSS_441	H12
BT13	VSS_359	VSS_442	H18
BT16	VSS_360	VSS_443	H22
BT18	VSS_361	VSS_444	H25
BT19	VSS_362	VSS_445	H32
BT21	VSS_363	VSS_446	H35
BT22	VSS_364	VSS_447	J10
BT23	VSS_365	VSS_448	J18
BT24	VSS_366	VSS_449	J22
BT25	VSS_367	VSS_450	J25
BT26	VSS_368	VSS_451	J32
BT27	VSS_369	VSS_452	J33
BT28	VSS_370	VSS_453	J36
BT29	VSS_371	VSS_454	J4
BT3	VSS_372	VSS_455	J7
BT33	VSS_373	VSS_456	K1
BT35	VSS_374	VSS_457	K10
BT38	VSS_375	VSS_458	K11
BT39	VSS_376	VSS_459	K2
BT4	VSS_377	VSS_460	K3
BT5	VSS_378	VSS_461	K38
BT6	VSS_379	VSS_462	K4
BT7	VSS_380	VSS_463	K5
BT8	VSS_381	VSS_464	K7
BT9	VSS_382	VSS_465	K8
BT10	VSS_383	VSS_466	K9
BT11	VSS_384	VSS_467	L29
BT12	VSS_385	VSS_468	L30
BT13	VSS_386	VSS_469	L33
BT14	VSS_387	VSS_470	L34
BT15	VSS_388	VSS_471	M12
BT16	VSS_389	VSS_472	M13
BT17	VSS_390	VSS_473	N10
BT18	VSS_391	VSS_474	N11
BT19	VSS_392	VSS_475	N12
BT20	VSS_393	VSS_476	N2
BT21	VSS_394	VSS_477	N12
BT22	VSS_395	VSS_478	N12
BT23	VSS_396	VSS_479	N12
BT24	VSS_397	VSS_480	N12
BT25	VSS_398	VSS_481	N12
BT26	VSS_399	VSS_482	N12
BT27	VSS_400	VSS_483	N12
BT28	VSS_401	VSS_484	N12
BT29	VSS_402	VSS_485	N12
BT30	VSS_403	VSS_486	N12
BT31	VSS_404	VSS_487	N12
BT32	VSS_405	VSS_488	N12
BT33	VSS_406	VSS_489	N12
BT34	VSS_407	VSS_490	N12
BT35	VSS_408	VSS_491	N12
BT36	VSS_409	VSS_492	N12
BT37	VSS_410	VSS_493	N12
BT38	VSS_411	VSS_494	N12
BT39	VSS_412	VSS_495	N12
BT40	VSS_413	VSS_496	N12
BT41	VSS_414	VSS_497	N12
BT42	VSS_415	VSS_498	N12
BT43	VSS_416	VSS_499	N12
BT44	VSS_417	VSS_500	N12
BT45	VSS_418	VSS_501	N12
BT46	VSS_419	VSS_502	N12
BT47	VSS_420	VSS_503	N12
BT48	VSS_421	VSS_504	N12
BT49	VSS_422	VSS_505	N12
BT50	VSS_423	VSS_506	N12
BT51	VSS_424	VSS_507	N12
BT52	VSS_425	VSS_508	N12
BT53	VSS_426	VSS_509	N12
BT54	VSS_427	VSS_510	N12
BT55	VSS_428	VSS_511	N12
BT56	VSS_429	VSS_512	N12
BT57	VSS_430	VSS_513	N12
BT58	VSS_431	VSS_514	N12
BT59	VSS_432	VSS_515	N12
BT60	VSS_433	VSS_516	N12
BT61	VSS_434	VSS_517	N12
BT62	VSS_435	VSS_518	N12
BT63	VSS_436	VSS_519	N12
BT64	VSS_437	VSS_520	N12
BT65	VSS_438	VSS_521	N12
BT66	VSS_439	VSS_522	N12
BT67	VSS_440	VSS_523	N12
BT68	VSS_441	VSS_524	N12
BT69	VSS_442	VSS_525	N12
BT70	VSS_443	VSS_526	N12
BT71	VSS_444	VSS_527	N12
BT72	VSS_445	VSS_528	N12
BT73	VSS_446	VSS_529	N12
BT74	VSS_447	VSS_530	N12
BT75	VSS_448	VSS_531	N12
BT76	VSS_449	VSS_532	N12
BT77	VSS_450	VSS_533	N12
BT78	VSS_451	VSS_534	N12
BT79	VSS_452	VSS_535	N12
BT80	VSS_453	VSS_536	N12
BT81	VSS_454	VSS_537	N12
BT82	VSS_455	VSS_538	N12
BT83	VSS_456	VSS_539	N12
BT84	VSS_457	VSS_540	N12
BT85	VSS_458	VSS_541	N12
BT86	VSS_459	VSS_542	N12
BT87	VSS_460	VSS_543	N12
BT88	VSS_461	VSS_544	N12
BT89	VSS_462	VSS_545	N12
BT90	VSS_463	VSS_546	N12
BT91	VSS_464	VSS_547	N12
BT92	VSS_465	VSS_548	N12
BT93	VSS_466	VSS_549	N12
BT94	VSS_467	VSS_550	N12
BT95	VSS_468	VSS_551	N12
BT96	VSS_469	VSS_552	N12
BT97	VSS_470	VSS_553	N12
BT98	VSS_471	VSS_554	N12
BT99	VSS_472	VSS_555	N12
BT100	VSS_473	VSS_556	N12
BT101	VSS_474	VSS_557	N12
BT102	VSS_475	VSS_558	N12
BT103	VSS_476	VSS_559	N12
BT104	VSS_477	VSS_560	N12
BT105	VSS_478	VSS_561	N12
BT106	VSS_479	VSS_562	N12
BT107	VSS_480	VSS_563	N12
BT108	VSS_481	VSS_564	N12
BT109	VSS_482	VSS_565	N12
BT110	VSS_483	VSS_566	N12
BT111	VSS_484	VSS_567	N12
BT112	VSS_485	VSS_568	N12
BT113	VSS_486	VSS_569	N12
BT114	VSS_487	VSS_570	N12
BT115	VSS_488	VSS_571	N12
BT116	VSS_489	VSS_572	N12
BT117	VSS_490	VSS_573	N12
BT118	VSS_491	VSS_574	N12
BT119	VSS_492	VSS_575	N12
BT120	VSS_493	VSS_576	N12
BT121	VSS_494	VSS_577	N12
BT122	VSS_495	VSS_578	N12
BT123	VSS_496	VSS_579	N12
BT124	VSS_497	VSS_580	N12
BT125	VSS_498	VSS_581	N12
BT126	VSS_499	VSS_582	N12
BT127	VSS_500	VSS_583	N12
BT128	VSS_501	VSS_584	N12
BT129	VSS_502	VSS_585	N12
BT130	VSS_503	VSS_586	N12
BT131	VSS_504	VSS_587	N12
BT132	VSS_505	VSS_588	N12
BT133	VSS_506	VSS_589	N12
BT134	VSS_507	VSS_590	N12
BT135	VSS_508	VSS_591	N12
BT136	VSS_509	VSS_592	N12
BT137	VSS_510	VSS_593	N12
BT138	VSS_511	VSS_594	N12
BT139	VSS_512	VSS_595	N12
BT140	VSS_513	VSS_596	N12
BT141	VSS_514	VSS_597	N12
BT142	VSS_515	VSS_598	N12
BT143	VSS_516	VSS_599	N12
BT144	VSS_517	VSS_600	N12
BT145	VSS_518	VSS_601	N12
BT146	VSS_519	VSS_602	N12
BT147	VSS_520	VSS_603	N12
BT148	VSS_521	VSS_604	N12
BT149	VSS_522	VSS_605	N12
BT150	VSS_523	VSS_606	N12
BT151	VSS_524	VSS_607	N12
BT152	VSS_525	VSS_608	N12
BT153	VSS_526	VSS_609	N12
BT154	VSS_527	VSS_610	N12
BT155	VSS_528	VSS_611	N12
BT156	VSS_529	VSS_612	N12
BT157	VSS_530	VSS_613	N12
BT158	VSS_531	VSS_614	N12
BT159	VSS_532	VSS_615	N12
BT160	VSS_533	VSS_616	N12
BT161	VSS_534	VSS_617	N12
BT162	VSS_535	VSS_618	N12
BT163	VSS_536	VSS_619	N12
BT164	VSS_537	VSS_620	N12
BT165	VSS_538	VSS_621	N12
BT166	VSS_539	VSS_622	N12
BT167	VSS_540	VSS_623	N12
BT168	VSS_541	VSS_624	N12
BT169	VSS_542	VSS_625	N12
BT170	VSS_543	VSS_626	N12
BT171	VSS_544	VSS_627	N12
BT172	VSS_545	VSS_628	N12
BT173	VSS_546	VSS_629	N12
BT174	VSS_547	VSS_630	N12
BT175	VSS_548	VSS_631	N12
BT176	VSS_549	VSS_632	N12
BT177	VSS_550	VSS_633	N12
BT178	VSS_551	VSS_634	N12
BT179	VSS_552	VSS_635	N12
BT180	VSS_553	VSS_636	N12
BT181	VSS_554	VSS_637	N12
BT182	VSS_555	VSS_638	N12
BT183	VSS_556	VSS_639	N12
BT184	VSS_557	VSS_640	N12
BT185	VSS_558	VSS_641	N12
BT186	VSS_559	VSS_642	N12
BT187	VSS_560	VSS_643	N12
BT188	VSS_561	VSS_644	N12
BT189	VSS_562	VSS_645	N12
BT190	VSS_563	VSS_646	N12
BT191	VSS_564	VSS_647	N12
BT192	VSS_565	VSS_648	N12
BT193	VSS_566	VSS_649	N12
BT194	VSS_567	VSS_650	N12
BT195	VSS_568	VSS_651	N12
BT196	VSS_569	VSS_652	N12
BT197	VSS_570	VSS_653	N12
BT198	VSS_571	VSS_654	N12
BT199	VSS_572	VSS_655	N12
BT200	VSS_573	VSS_656	N12
BT201	VSS_574	VSS_657	N12
BT202	VSS_575	VSS_658	N12
BT203	VSS_576	VSS_659	N12
BT204	VSS_577	VSS_660	N12
BT205	VSS_578	VSS_661	N12
BT206	VSS_579	VSS_662	N12
BT207	VSS_580	VSS_663	N12
BT208	VSS_581	VSS_664	N12
BT209	VSS_582	VSS_665	N12
BT210	VSS_583	VSS_666	N12
BT211	VSS_584	VSS_667	N12
BT212	VSS_585	VSS_668	N12
BT213	VSS_586	VSS_669	N12
BT214	VSS_587	VSS_670	N12
BT215	VSS_588	VSS_671	N12
BT216	VSS_589	VSS_672	N12
BT217	VSS_590	VSS_673	N12
BT218	VSS_591	VSS_674	N12
BT219	VSS_592	VSS_675	N12
BT220	VSS_593	VSS_676	N12
BT221	VSS_594	VSS_677	N12
BT222	VSS_595	VSS_678	N12
BT223	VSS_596	VSS_679	N12
BT224	VSS_597	VSS_680	N12
BT225	VSS_598	VSS_681	N12
BT226	VSS_599	VSS_682	N12
BT227	VSS_600	VSS_683	N12
BT228	VSS_601	VSS_684	N12
BT229	VSS_602	VSS_685	N12
BT230	VSS_603	VSS_686	N12
BT231	VSS_604	VSS_687	N12
BT232	VSS_605	VSS_688	N12
BT233	VSS_606	VSS_689	N12
BT234	VSS_607	VSS_690	N12
BT235	VSS_608	VSS_691	N12
BT236	VSS_609	VSS_692	N12
BT237	VSS_610	VSS_693	N12
BT238	VSS_611	VSS_694	N12
BT239	VSS_612	VSS_695	N12
BT240	VSS_613	VSS_696	N12
BT241	VSS_614	VSS_697	N12
BT242	VSS_615	VSS_698	N12
BT243	VSS_616	VSS_699	N12
BT244	VSS_617	VSS_700	N12
BT245	VSS_618	VSS_701	N12
BT246	VSS_619	VSS_702	N12
BT247	VSS_620	VSS_703	N12
BT248	VSS_621	VSS_704	N12
BT249	VSS_622	VSS_705	N12
BT250	VSS_623	VSS_706	N12
BT251	VSS_624	VSS_707	N12
BT252	VSS_625	VSS_708	N12
BT253	VSS_626	VSS_709	N12
BT254	VSS_627	VSS_710	N12
BT255	VSS_628	VSS_711	N12
BT256	VSS_629	VSS_712	N12
BT257	VSS_630	VSS_713	N12
BT258	VSS_631	VSS_714	N12
BT259	VSS_632	VSS_715	N12
BT260	VSS_633	VSS_716	N12
BT261	VSS_634	VSS_717	N12
BT262	VSS_635	VSS_718	N12
BT263	VSS_636	VSS_719	N12
BT264	VSS_637	VSS_720	N12
BT265	VSS_638	VSS_721	N12
BT266	VSS_639	VSS_722	

DDR4 SO-DIMM A

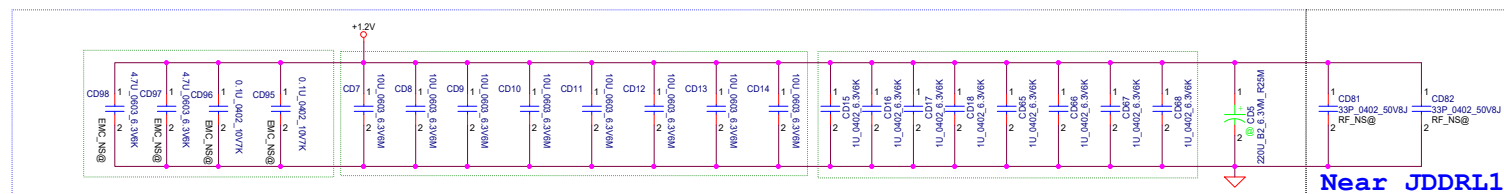
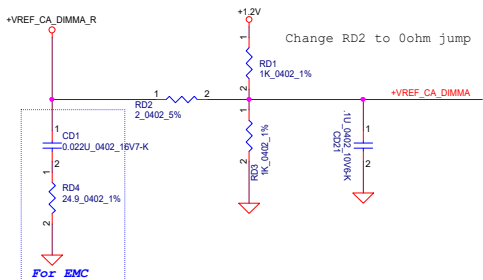
Layout Note:
Place near DIMM




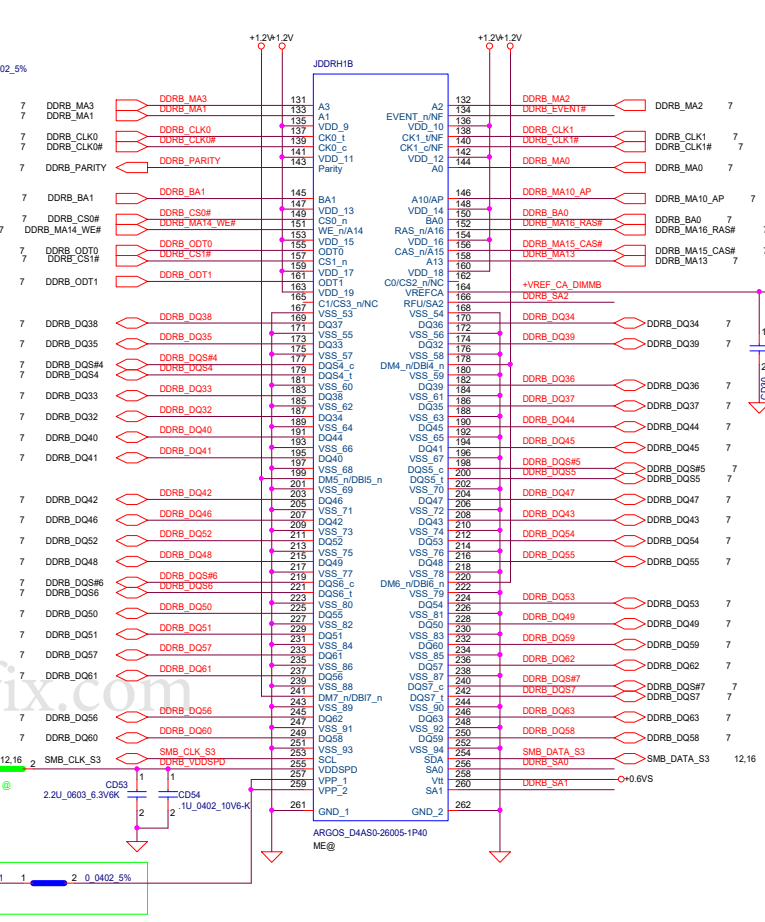
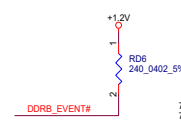
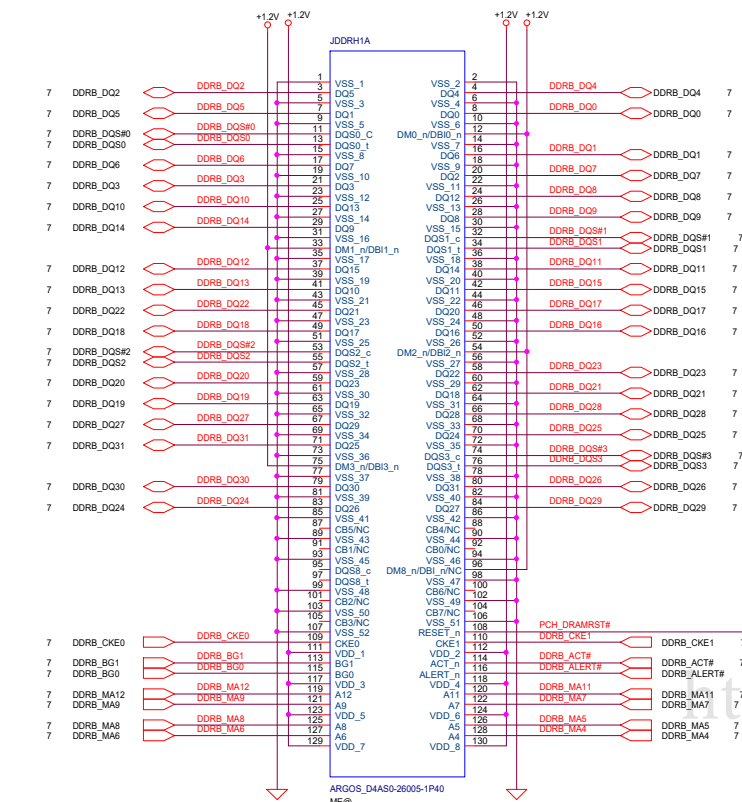
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM socket

SPD Address = 0H

Layout Note:
Place near DIMM

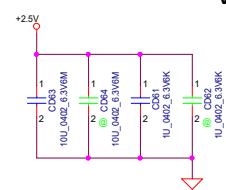
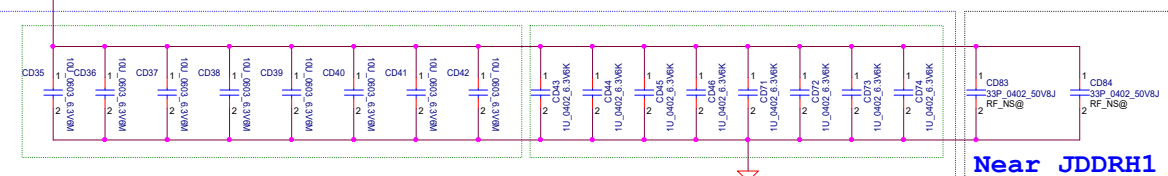
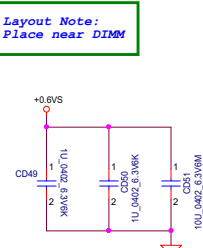


Security Classification	LC Future Center Secret Data			Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	DDRVI SO-DIMM A	
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Size	Document Number			Rev	
	Y540			2.0	
Date:	Friday, March 22, 2019			Sheet	12 of 77

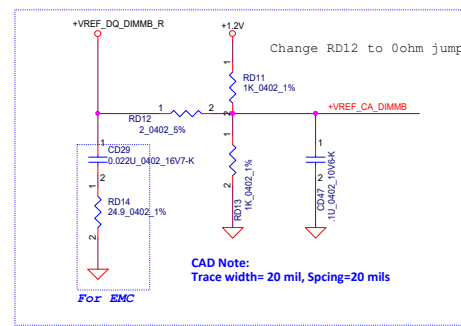
DDR4 SO-DIMM B


SPD Address = 2H

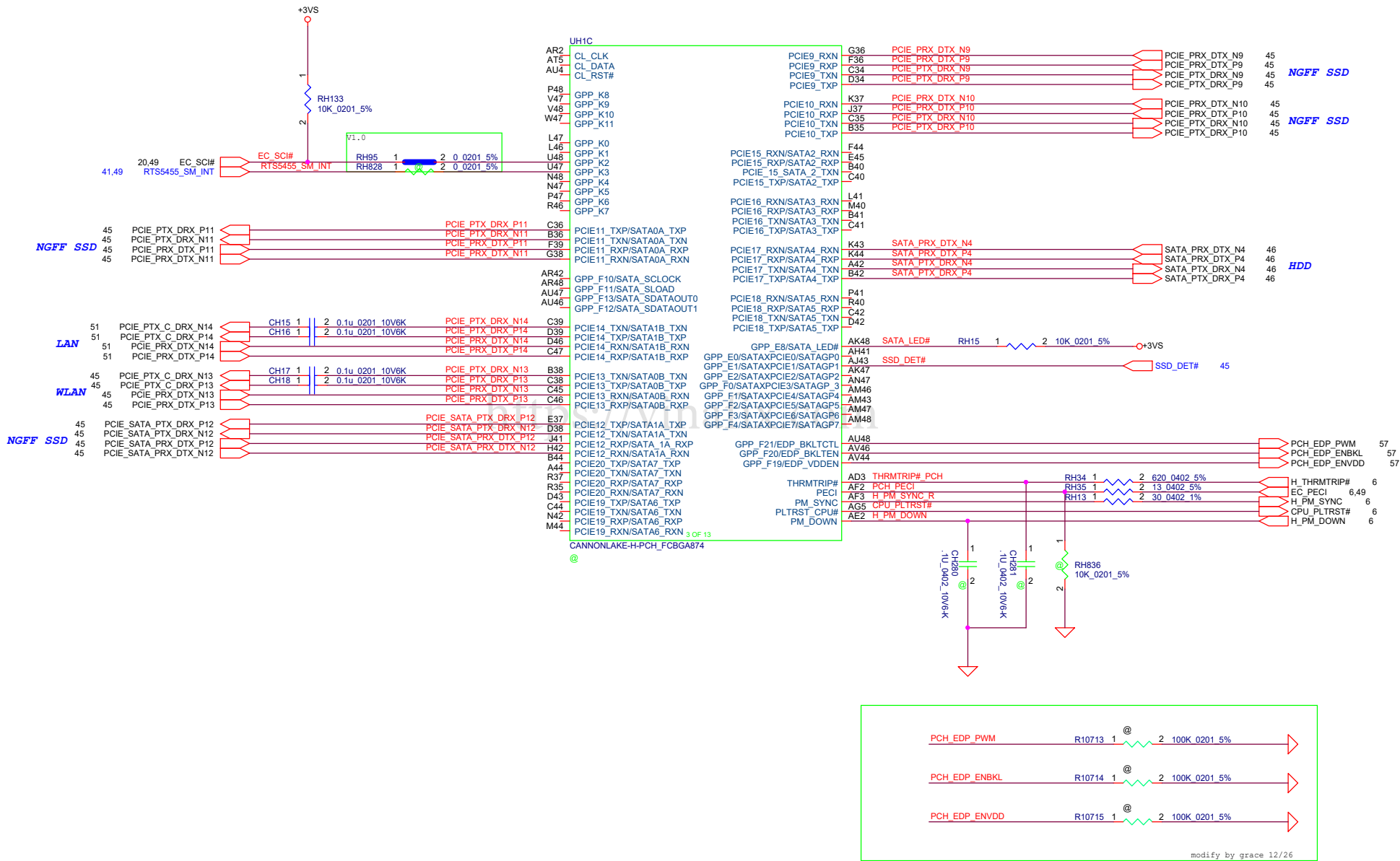
Layout Note:
Place near DIMM




Near JDDRH1



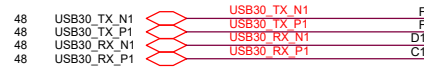
Security Classification		LC Future Center Secret Data		Title		
Issued Date		Deciphered Date		2018/08/02		
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Issued Date	2018/08/02	Deciphered Date	2018/08/02	PCH (1/9) PCle/SATA/GPPFG		
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HM370 only have 4(#1-#4) USB3.1 GEN2 port

Back USB (3.0)



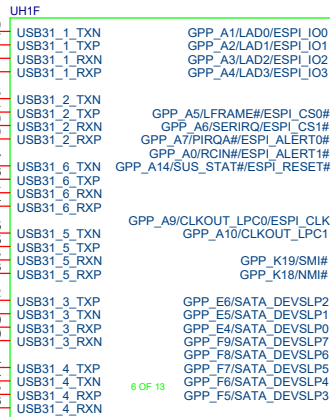
TYPE-C USB (3.0)



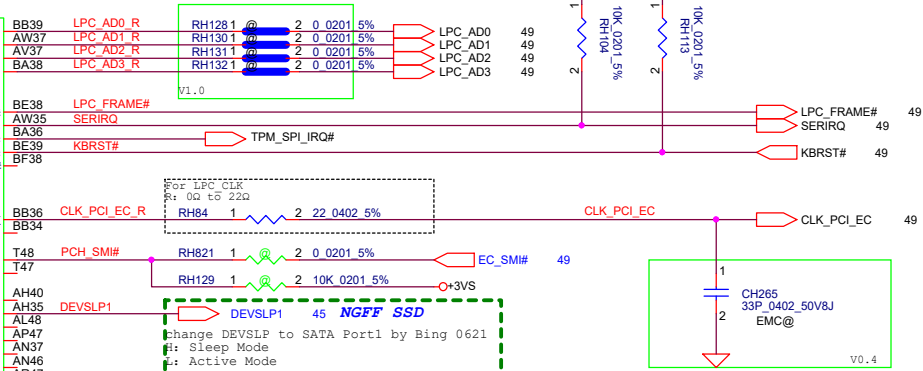
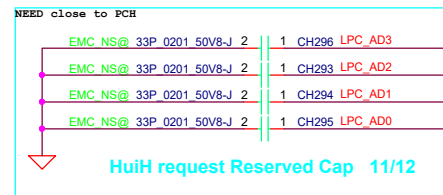
LEFT USB (3.0)
MB(AOU)



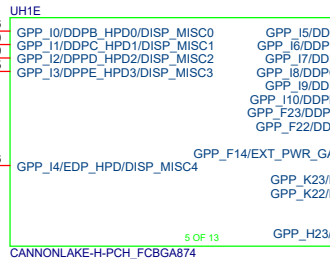
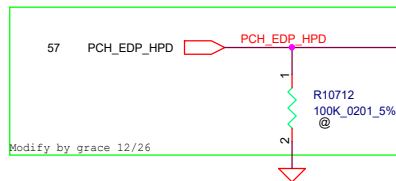
Right USB (3.0)
DB



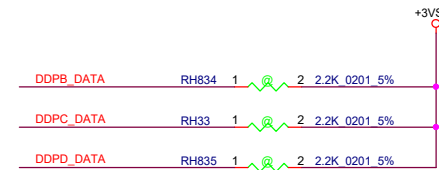
CANNONLAKE-H-PCH_FCBGA874




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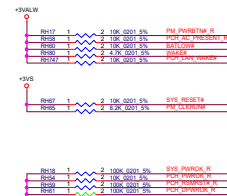
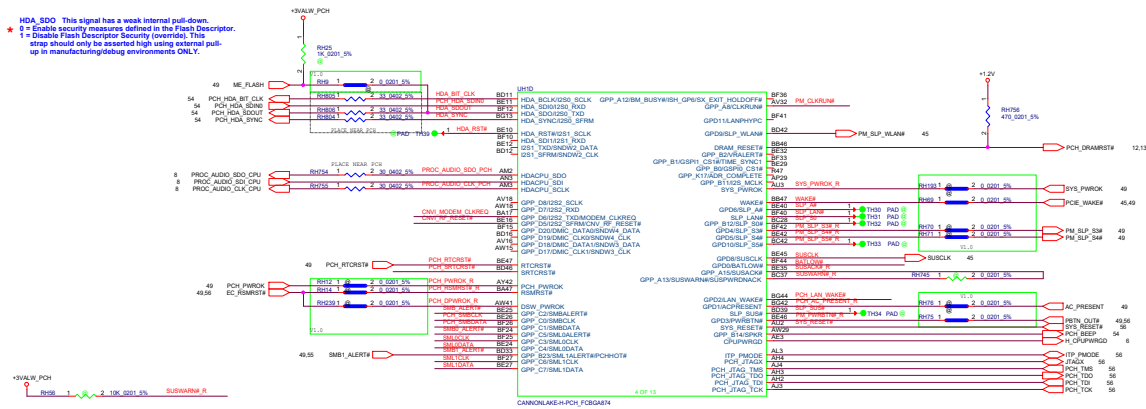
CANNONLAKE-H-PCH_FCBGA874



- DDPB_CTRLDATA**
The signal has a weak internal pull-down.
H Port B is detected.
* L Port B is not detected.
- DDPC_CTRLDATA**
The signal has a weak internal pull-down.
* H Port C is detected.
L Port C is not detected. (Default)
- DDPD_CTRLDATA**
The signal has a weak internal pull-down.
H Port D is detected.
* L Port D is not detected. (Default)

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★ **HDA_SDO** This signal has a weak internal pull-down.
 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

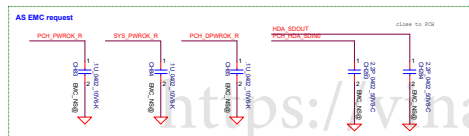
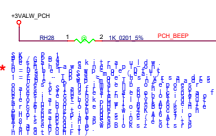
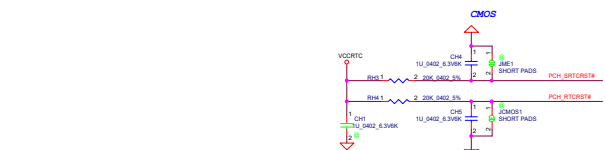


GPP_C2 / \$MBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

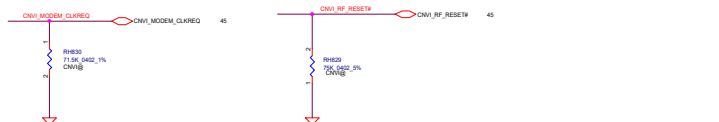
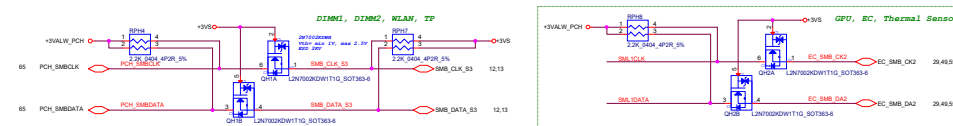
GPP_C5 / \$MLOALERT#
This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).

GPP_B23 / \$M1ALERT# / PCH#HOT#
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB

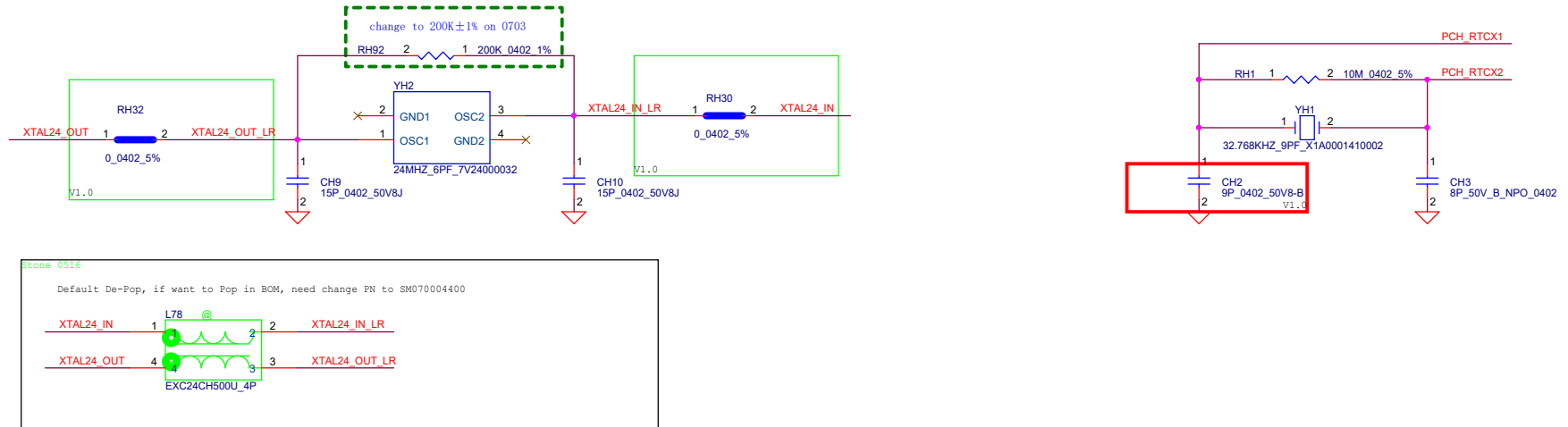
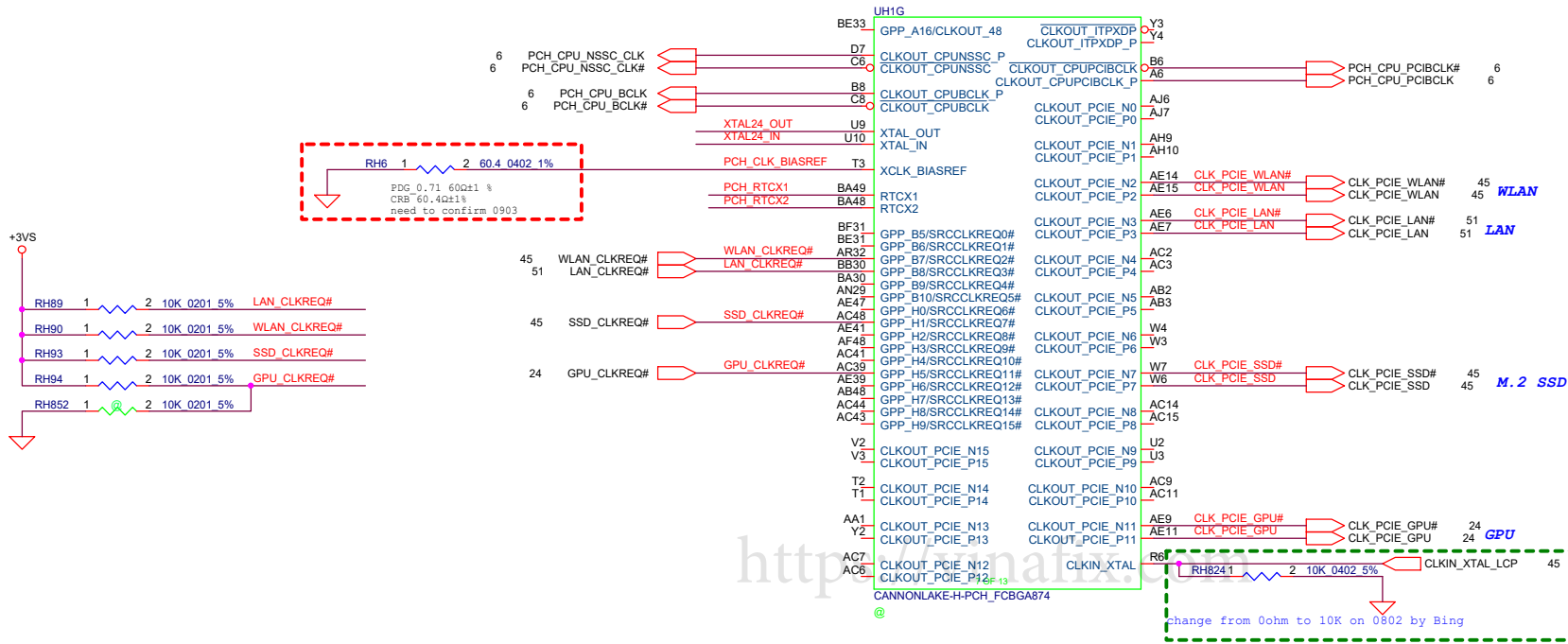
Note: When used as PCH#HOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down.




RSMRST# sequence control circuit

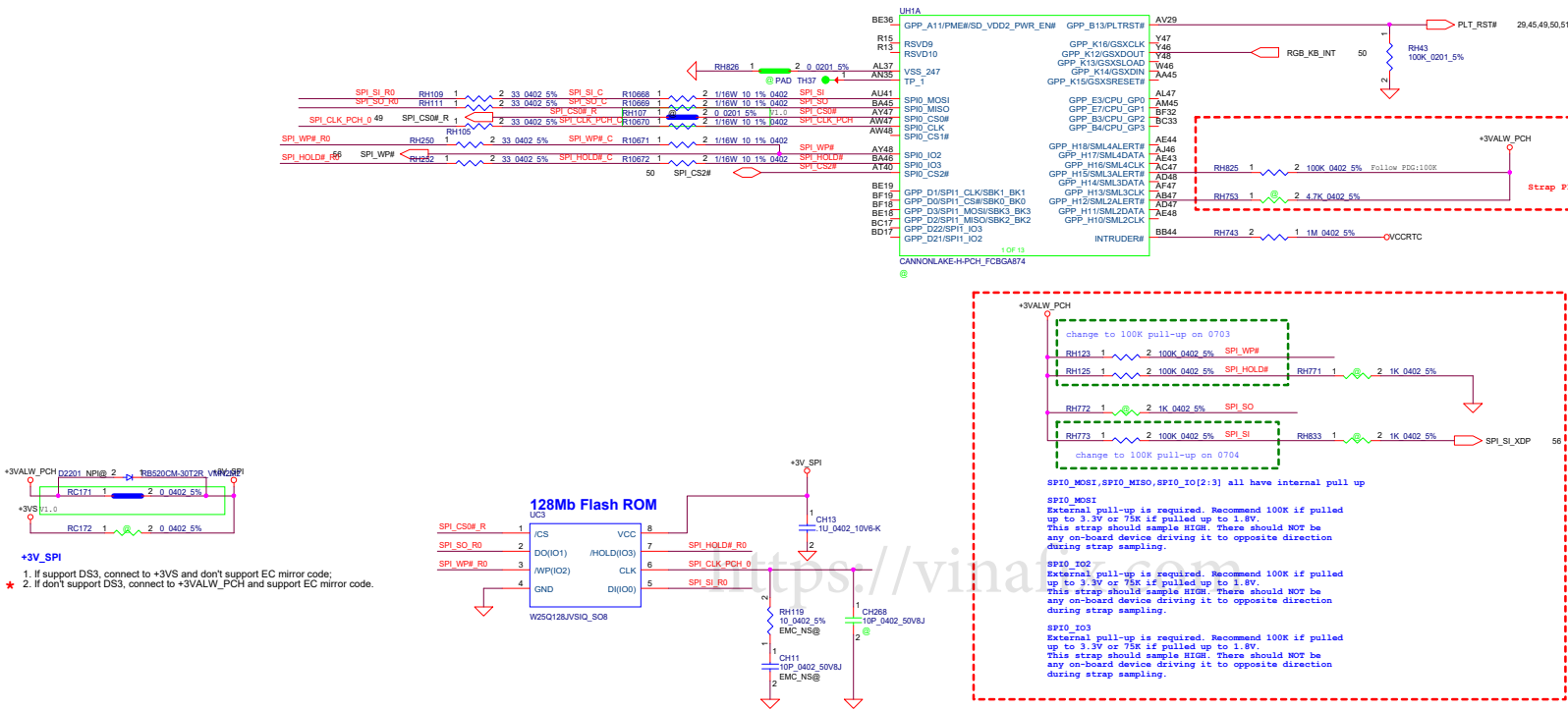


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Date		Printed	1 of 2



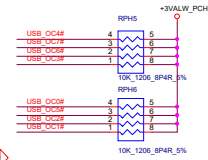
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	PCH (3/9) CLOCK, GPPBH	
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PCH (3/9) CLOCK,GPPBH		LCFC	
Y540			



+3V_SPI

1. If support DS3, connect to +3VS and don't support EC mirror code.
★ 2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.



Need to confirm with Intel 0526@stone

+1.8V_{ALV}

Timing diagram for Strap Pin showing signals RH815, RH809, RH810, RH808, and RH807. The diagram includes a red arrow pointing to the RH815 signal and a red arrow pointing to the RH808 signal. The signals are labeled with their names, widths, delays, and percentages.

Signal	Width	Delay	Percentage
RH815	2	10K 0201 5%	GPP J4
RH809	2	2.2K 0402 5%	GPP J6
RH810	2	2.2K 0402 5%	GPP J6
RH808	1	2.2K 0402 5%	GPP J6
RH807	2	2.2K 0201 5%	GPP J6

Strap Pin


[illegible]

CAD Note:
Trace width=15 mils, Spacing=15mil
Max length=N/A mils.

02 Stone: Add refer to EDS&CRB

5.4 GPPJ_RCOMP_1P8 Signal

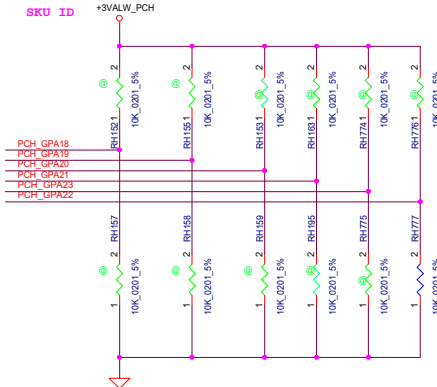
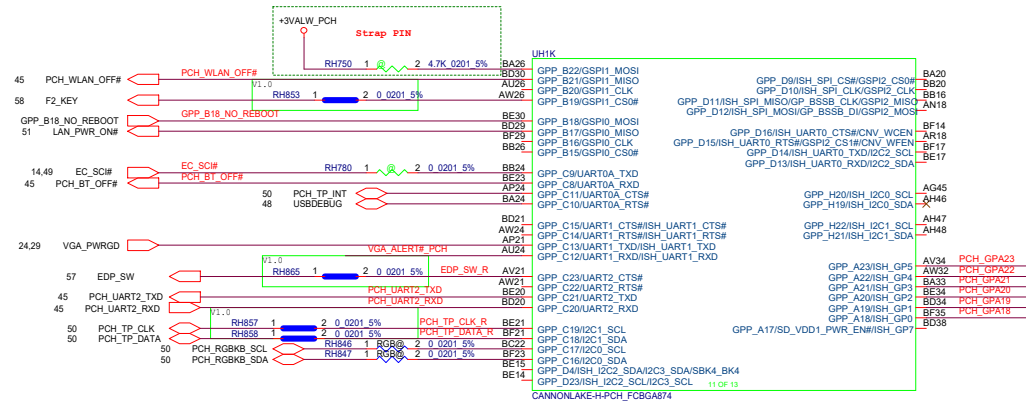
The PCB implements the GPPJ_RCOMP_1P8 as an external bias resistor to ground. 200 Ohm ($\pm 1\%$) resistor to ground is required on the signal and this single resist can be shared with SGT1_RCOMP_3P0 and SGT1_RCOMP_1P0 on the platform.

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Issue		Document Number		Revision		Date			
Customer		Y540		Rev		2.0			
Order		Y540, March 22, 2019		Sheet		19		of 77	

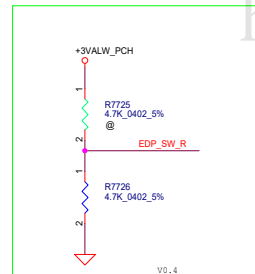
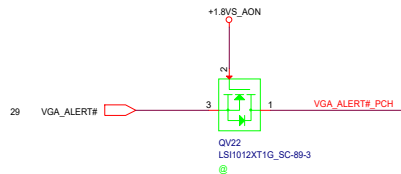


GPP_B22 /GSP11_MOSI (Boot BIOS Strap Bit BBS)
This signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset Dch, bit6)
0: SPI (default)
1: LPC
Notes:
1. The internal pull-down is disabled after PCH_PWRON is high.
4. This signal is in the primary well.

Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC

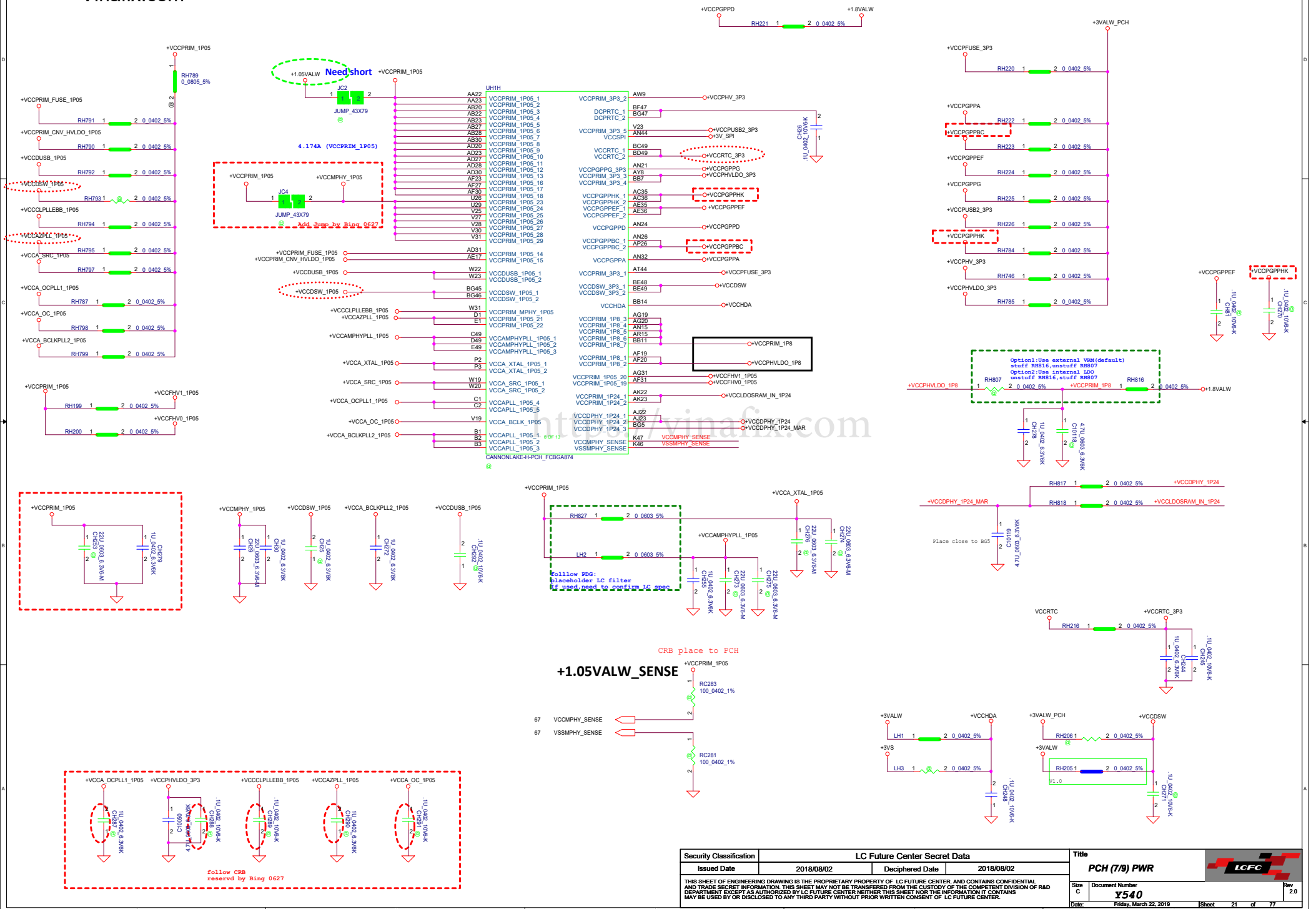


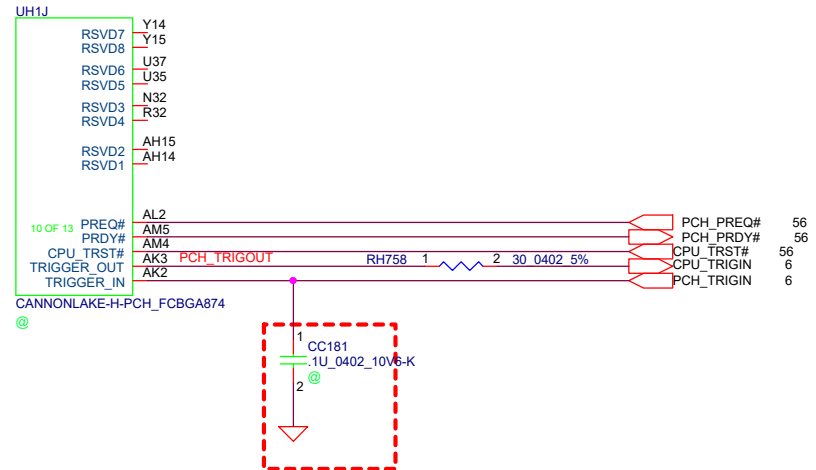
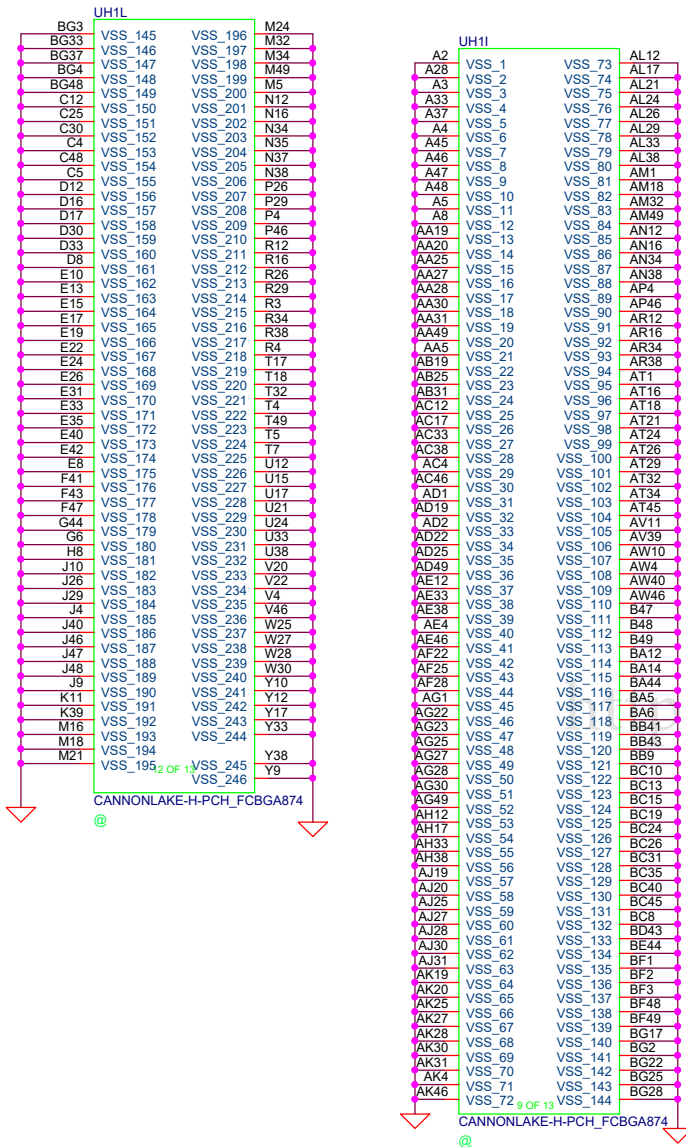
50 PCH_RGKB_SDA




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Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22	PCH_GPA23
Y540-15-N17P	0	0	0	0	X	X
Y540-15-N18E G0	0	0	0	1	X	X
Y540-15-N18E G1	0	0	1	0	X	X
Y540-15-N18P	0	0	1	1	X	X
Y7000P-15-N17P	0	1	0	0	X	X
Y7000P-15-N18E G0	0	1	0	1	X	X
Y7000P-15-N18E G1	0	1	1	0	X	X
Y7000P-15-N18P	0	1	1	1	X	X
Y540-17-N17P	1	0	0	0	X	X
Y540-17-N18E G0	1	0	0	1	X	X
Y540-17-N18E G1	1	0	1	0	X	X
Y540-17-N18P	1	0	1	1	X	X



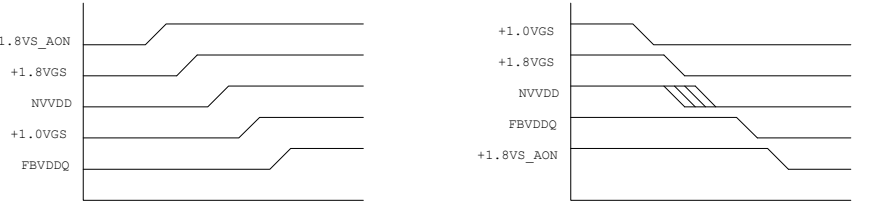


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N18E-G1 GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVDD_PWM_VID	PWM Output to control NVDD	NVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	GC6 FRAME BUFFER ENABLE	FB_GC6_EN	(10K pull down)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K pull High)
GPIO3	OUT	UNUSED	UNUSED	UNUSED	
GPIO4	OUT	GC6:1V8_MAIN_EN	GPU power sequencing for GC6 --- 1V8_MAIN_EN	1V8_MAIN_EN	(10K pull High)
GPIO5	IN	FRAME_LOCK*	Active low Frame Lock for NVSR panel	GPU_FRAME_LOCK#	
GPIO6	OUT	NVDD_PSI*	Phase Shedding, NVDD_PSI	NVDD_PSI	(5.1K pull High)
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K pull down)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K pull down)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K pull High)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF	(10K pull down)
GPIO11	OUT	LCD_VCC	LCD Panel VOLTAGE	GPU_EDP_ENVDD	(10K pull down)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K pull High)
GPIO13	OUT	UNUSED	UNUSED	UNUSED	
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K pull High)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	UNUSED	
GPIO16	OUT	UNUSED	UNUSED	UNUSED	
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_ENBKL	(100K pull down)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	IFPE_HPD	(10K pull High)
GPIO19	OUT	Reserved	UNUSED	UNUSED	
GPIO20	OUT	GC6:NB_FGC6	Low Power States Fast CG6	NB_FGC6	(10K pull down)
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	
GPIO22		UNUSED	UNUSED	UNUSED	
GPIO23		UNUSED	UNUSED	RASTER_SYNC1	(100K pull down)
GPIO24	IN	HPD_IFPF*/USBC_HPD* or Dongle_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K pull High)
GPIO26		FP_FUSE	Field-programming of select fuses	GPIO26_FP_FUSE	(10K pull down)
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K pull High)
GPIO28		ADC_MUX_SEL	OVRM MUX SEL	ADC_MUX_SEL_R	(10K pull High)
GPIO29	OUT	IDLE_IN_SW	IDLE_IN_SW	IDLE_IN_SW	(10K pull down)
GPIO30		UNUSED	UNUSED	UNUSED	

N18E-G1 Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.

2. Delay from 1V8_MAIN_EN to PEXVDD/NVDD_PG0OD must NOT exceed 4ms.

3. It is recommended that the delay from 1V8_AON on to PEXVDD/NVDD_PG0OD assertion not exceed 20ms.

4. Power up NVDD must be 90% before PEXVDD can start ramp-up.

5. All 3.3V devices that connect to the GPU must be powered after 1V8_AON;GPU cannot have any 3.3V leakage paths before 1V8_AON is present.

6. Refer to the JEDEC Memory SPEC for memory-related power sequencing.

7. FBVDD/Q, USB_VDDP and 1V8_AON don't need power cycle for GC6
1. PEXVDD must power down before NVDD,

2. For GDDR6, VPP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed

3. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

4. Power down of PEXVDD must be less than 10% before NVDD can start ramp-down..

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

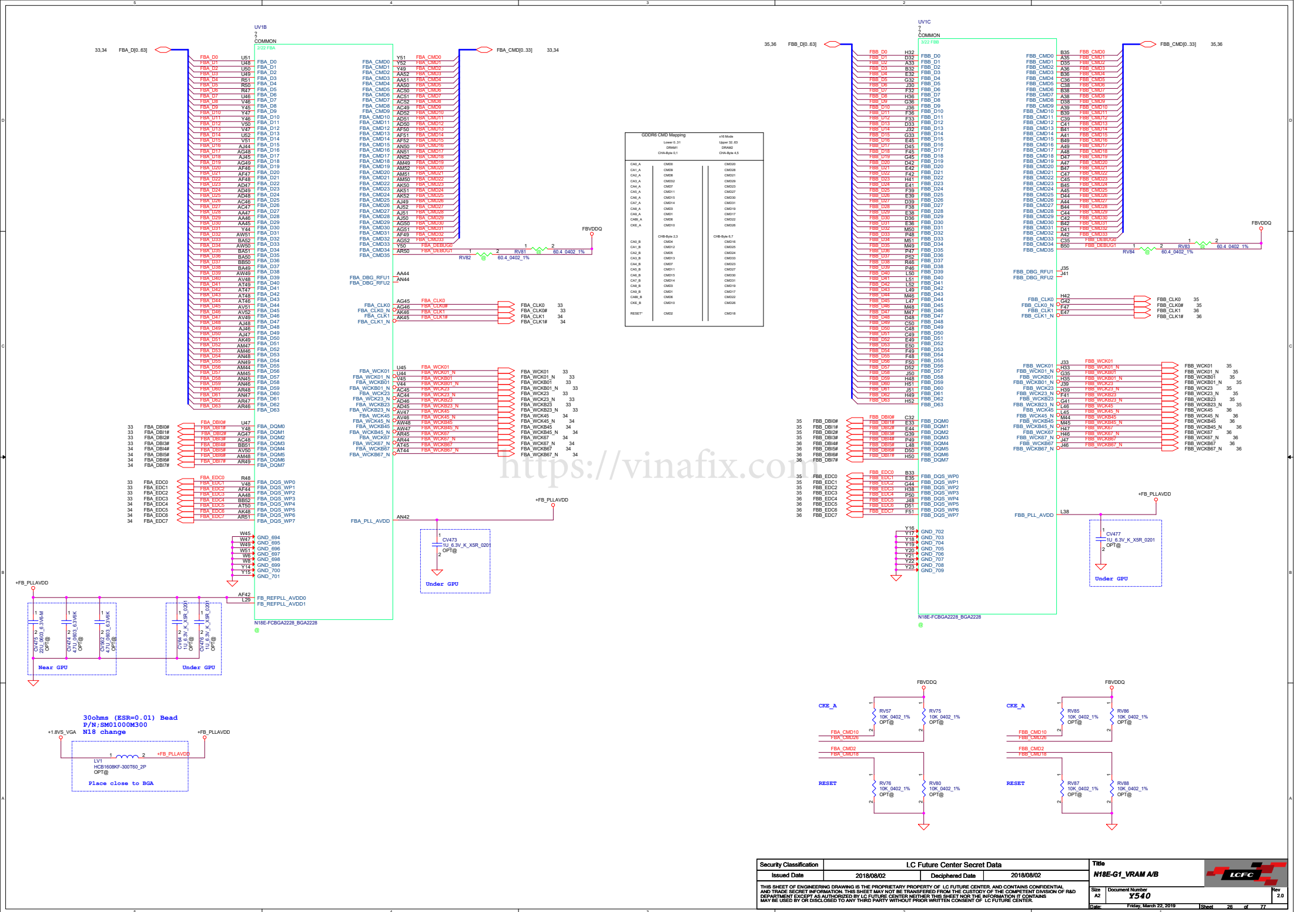
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	N18E-G1 VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14:A
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

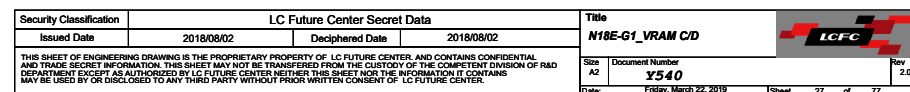
FS_OVERT# FUNCTION

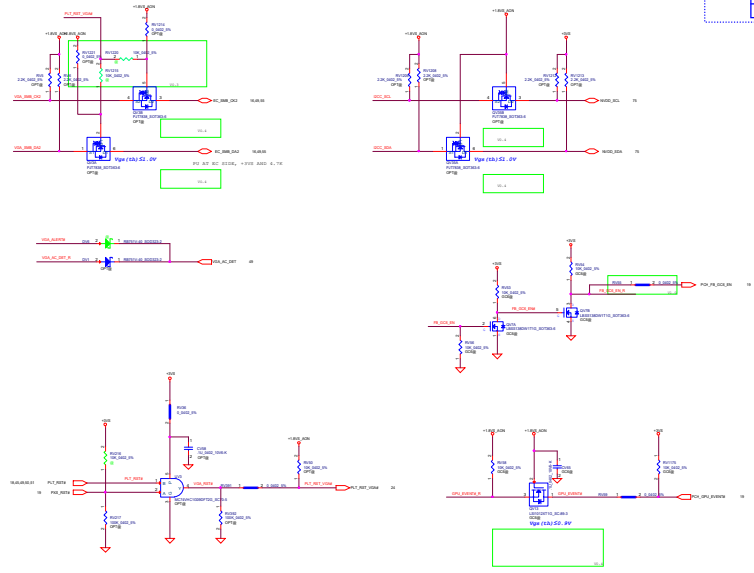
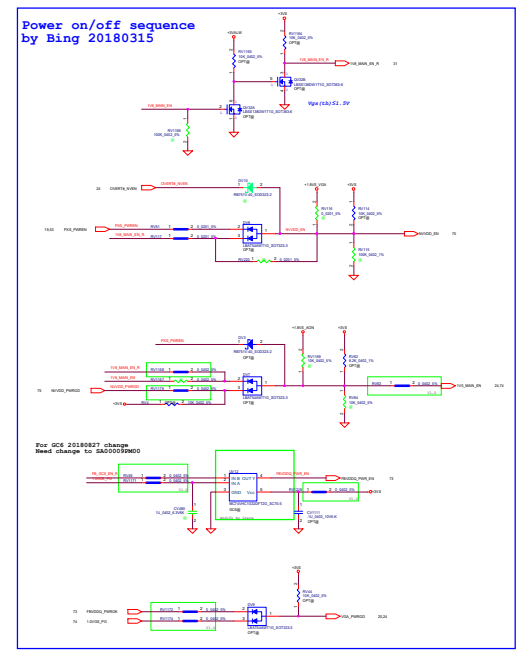
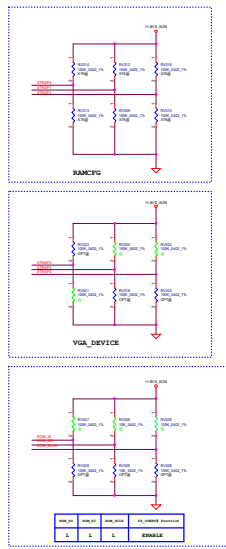
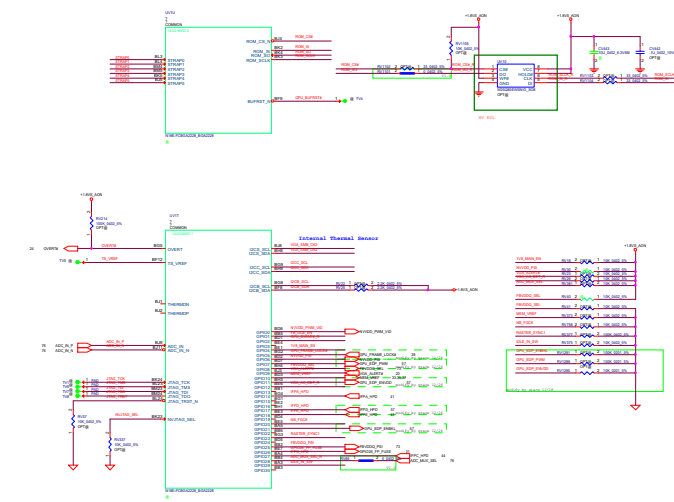
ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	L	FS_OVERT# function ENABLE
L	L	H	FS_OVERT# function DISABLED Reserved; do not configure

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL
- 1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





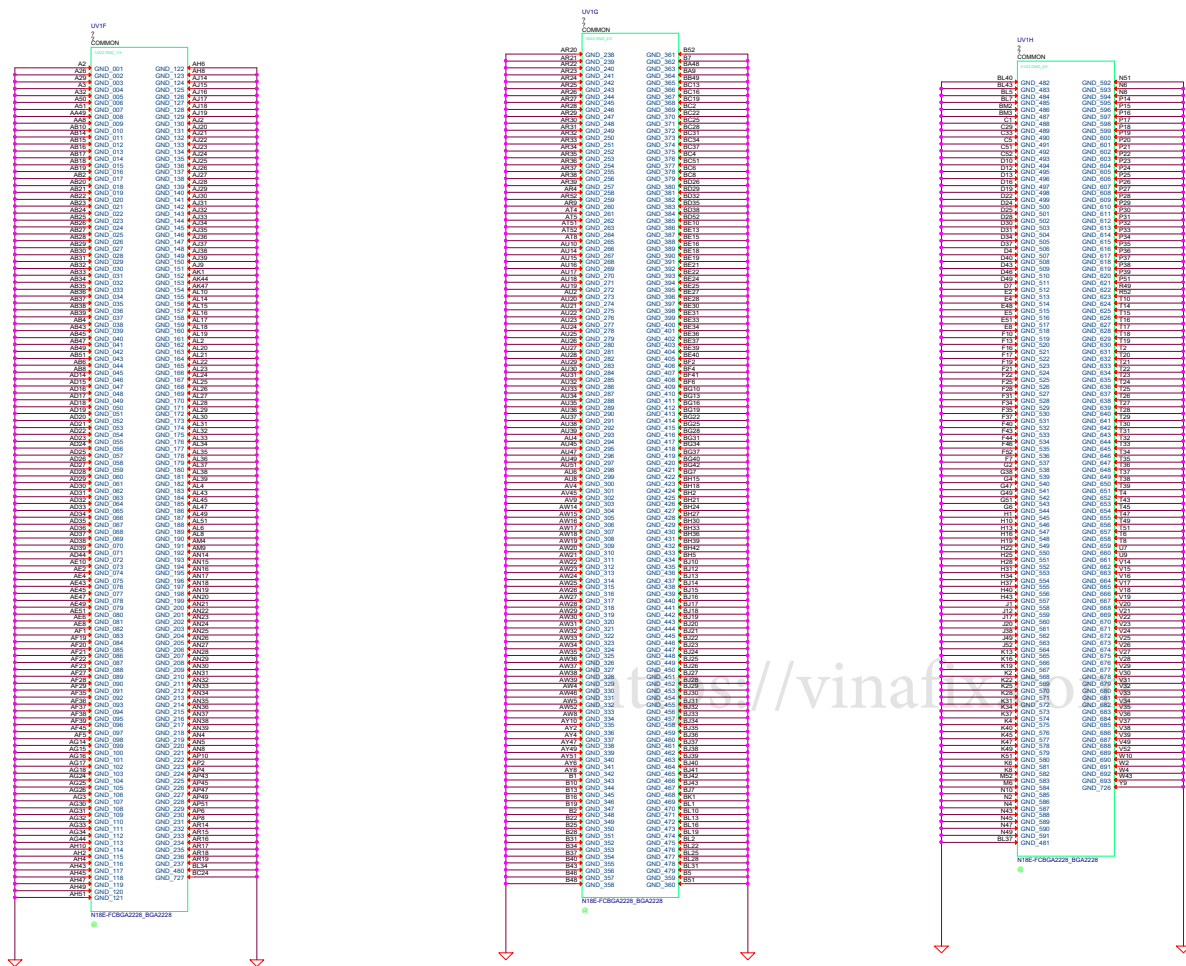


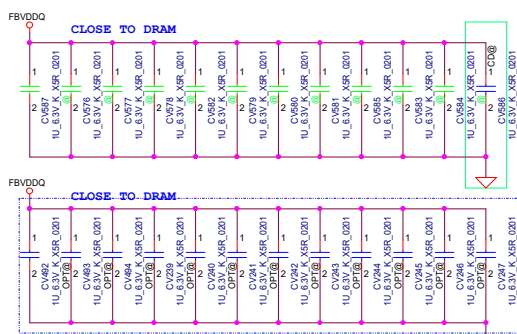
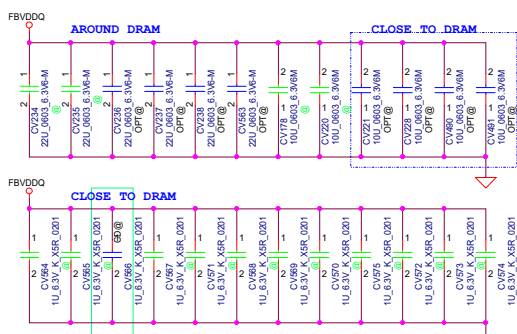
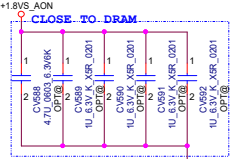
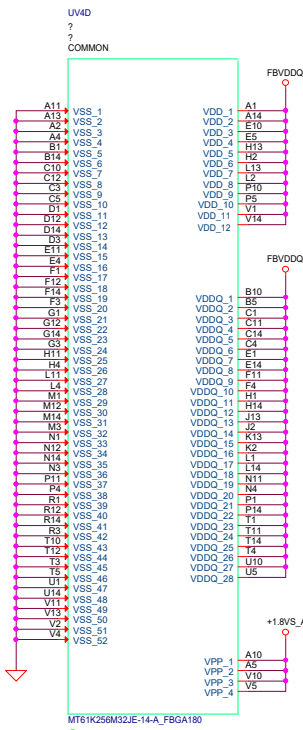
<https://vinafix.com>

Y540 N18E	Strap5	Strap4	Strap3
DGPU only+Non G-sync panel	0	0	1
DGPU only+G-sync panel	1	0	1

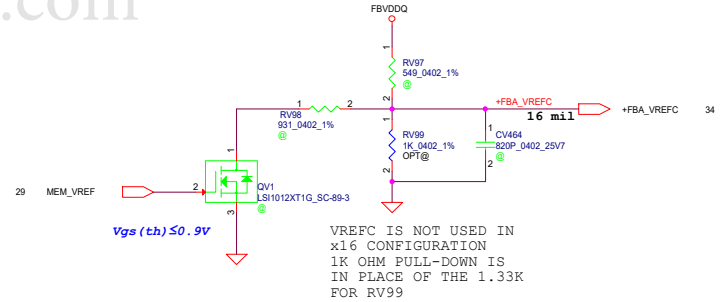
Key Specifications:			
	N18E-G3	N18E-G2	N18E-G1
Product Part Number	N18E-G3-A1	N18E-G2-A1	N18E-G1-KD-A1
NVIDIA Part Number ¹ (used on labels of packaging materials)	TU104-750-A1	TU106-750-A1	TU106-725-KD-A1
Device ID	<ul style="list-style-type: none"> Primary: 0x1E90 Secondary: 0x1ED0 	<ul style="list-style-type: none"> Primary: 0x1F10 Secondary: 0x1F50 	<ul style="list-style-type: none"> Primary: 0x1F11 Secondary: 0x1F51
Memory interface	256-bit GDDR6	256-bit GDDR6	192-bit GDDR6
Package	GB4B-256	GB4B-256	GB4B-256

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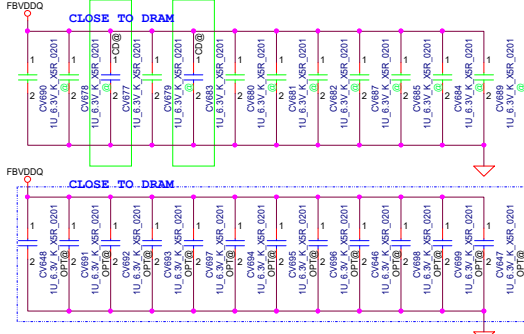
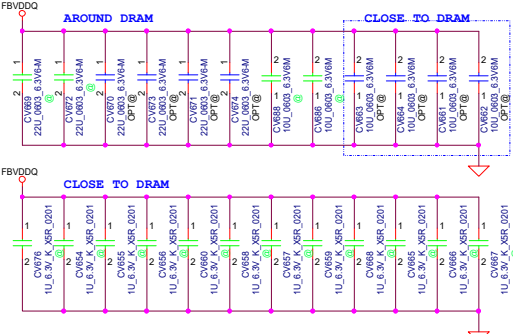
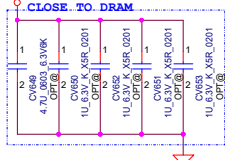
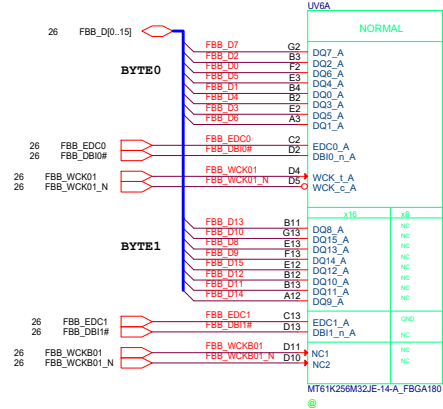
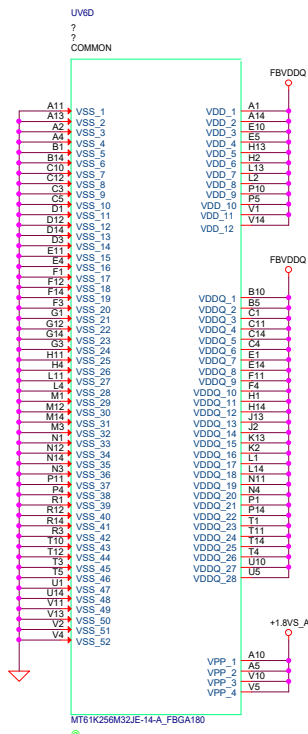




<https://vinafix.com>

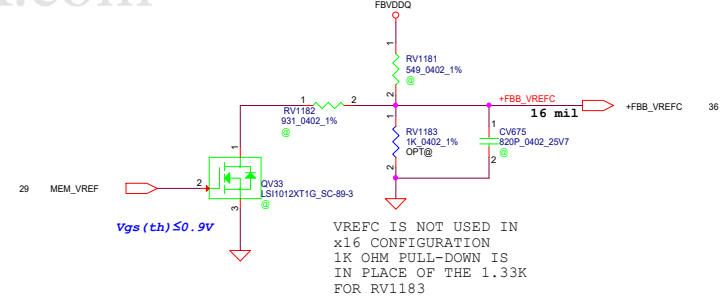
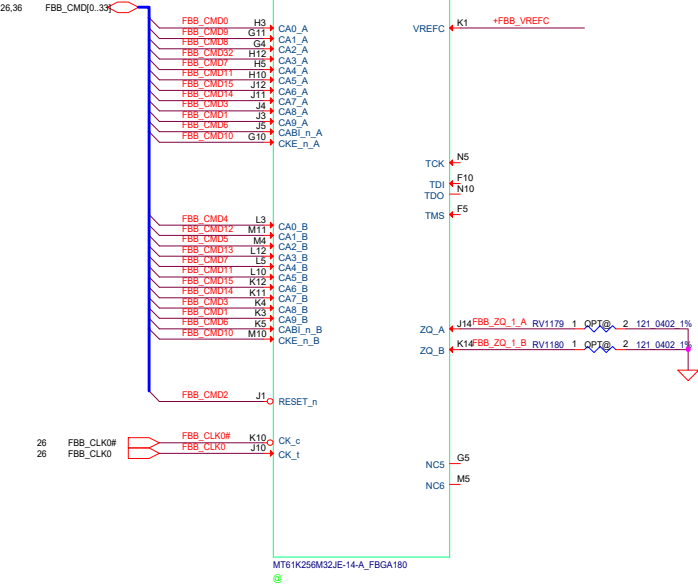
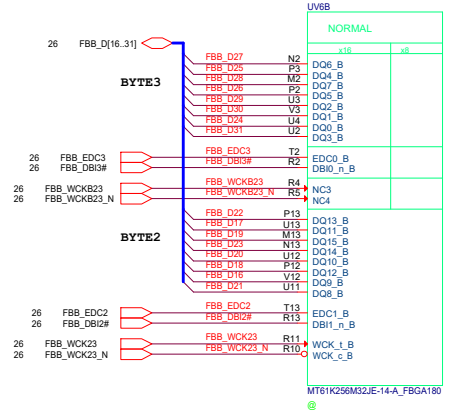


Vinafix.com

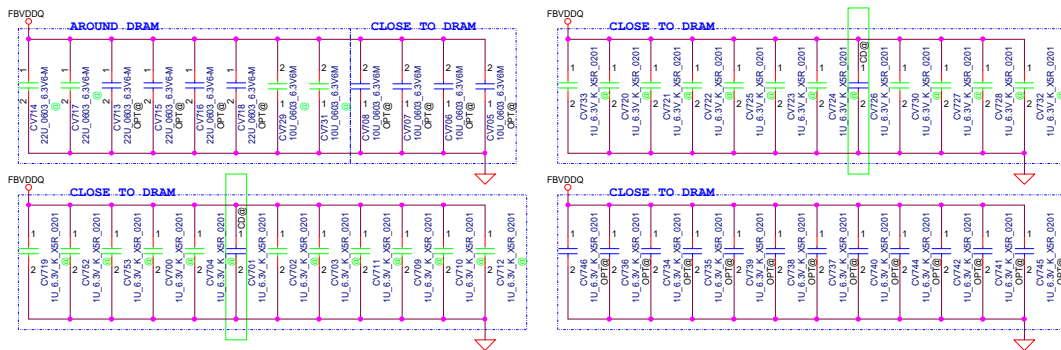
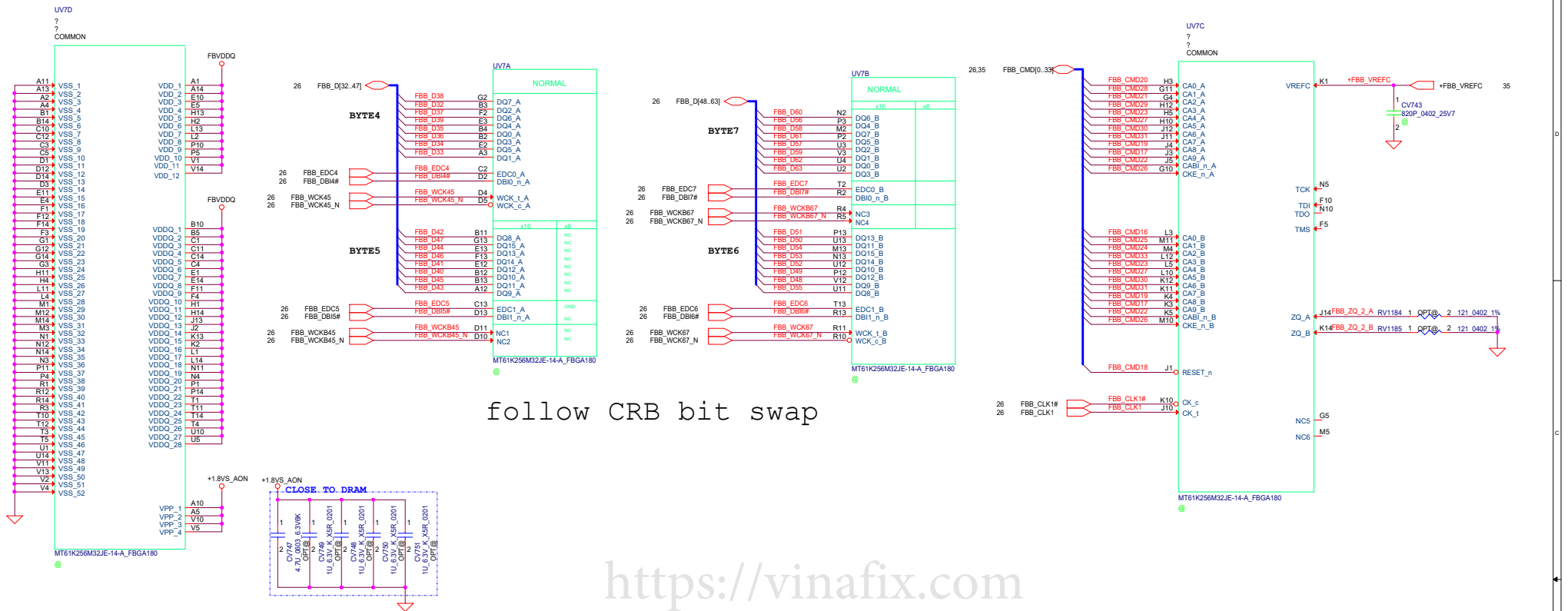


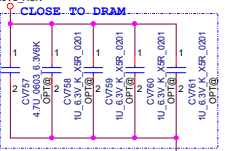
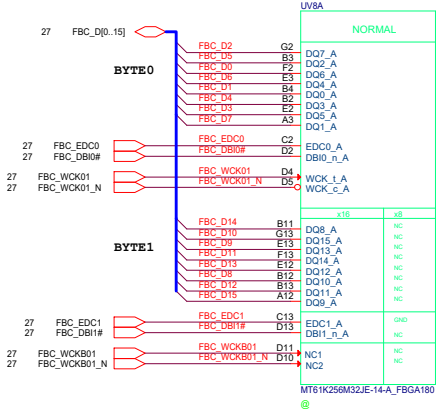
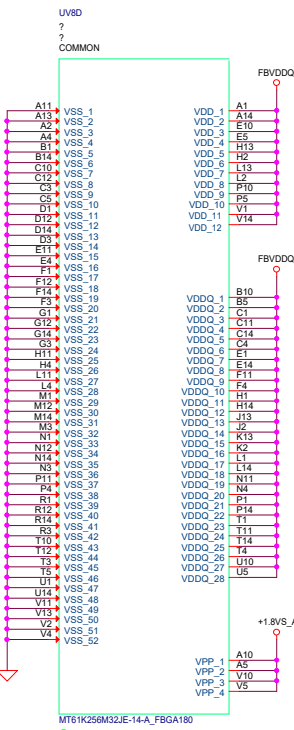
follow CRB bit swap

<https://vinafix.com>



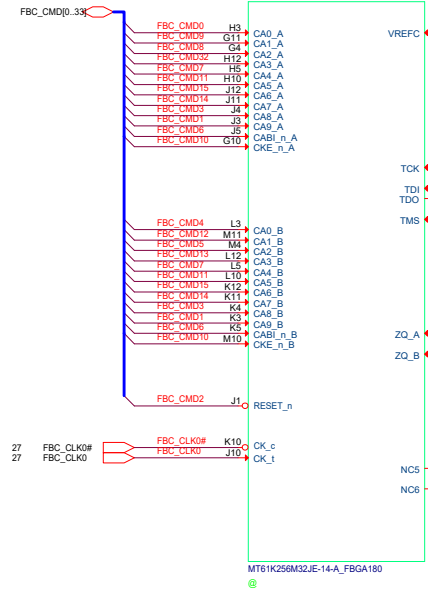
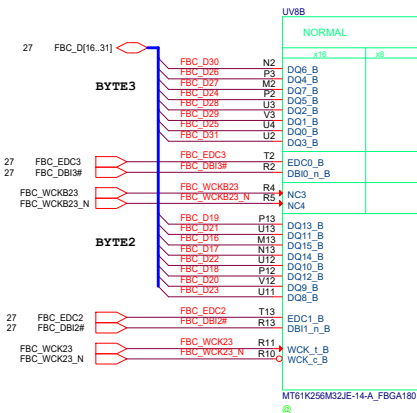
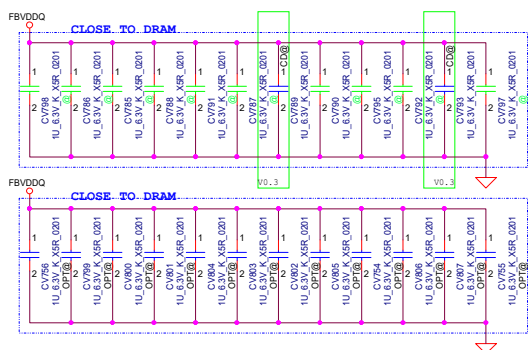
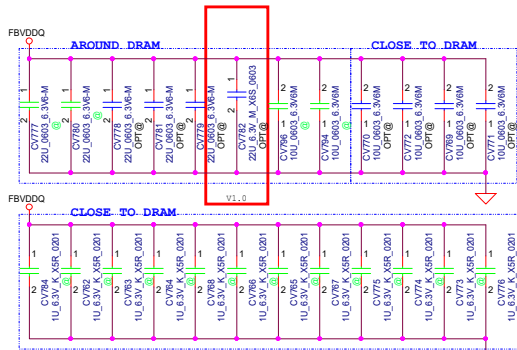
VREFC IS NOT USED IN x16 CONFIGURATION 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR RV1183



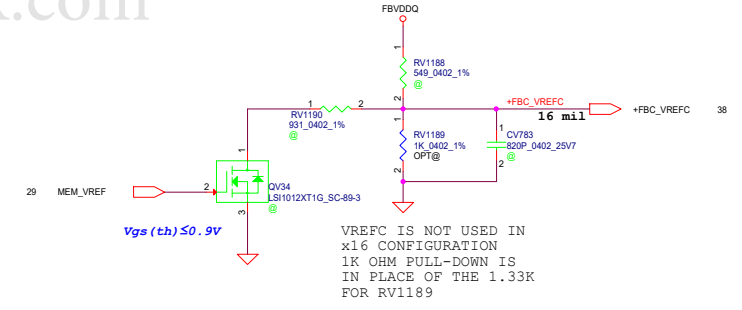


follow CRB bit swap

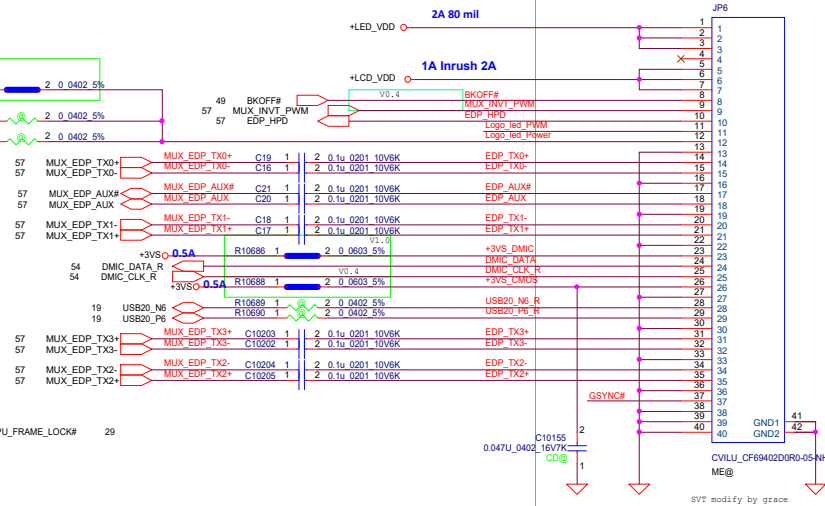
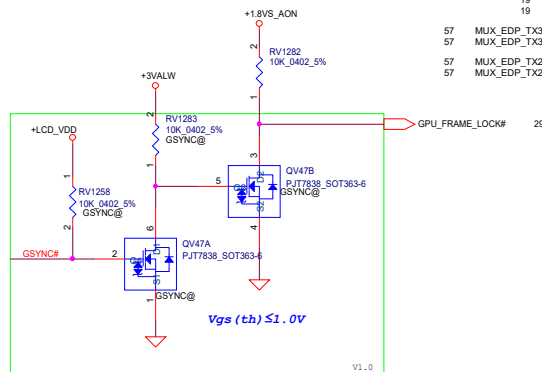
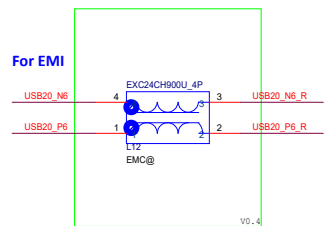
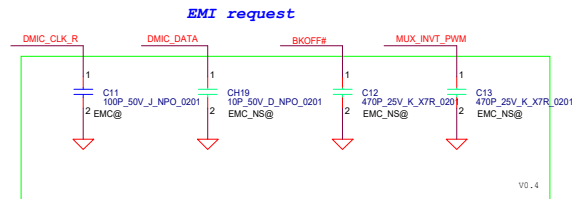
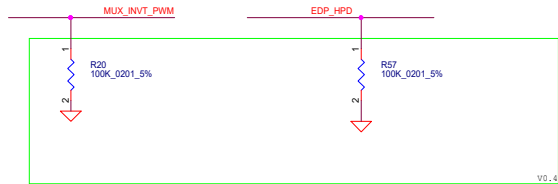
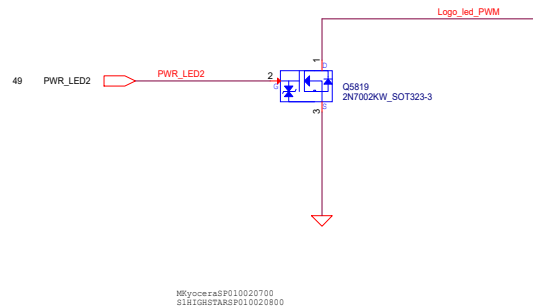
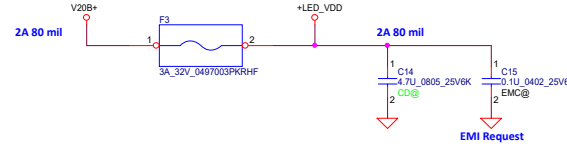
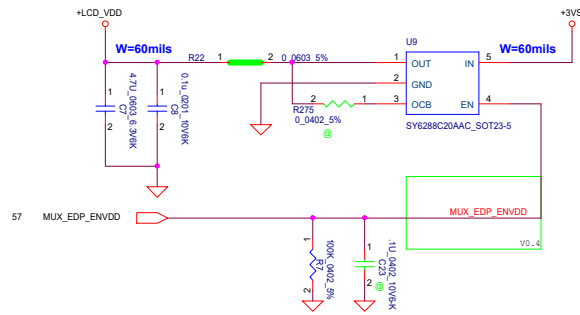
<https://vinafix.com>



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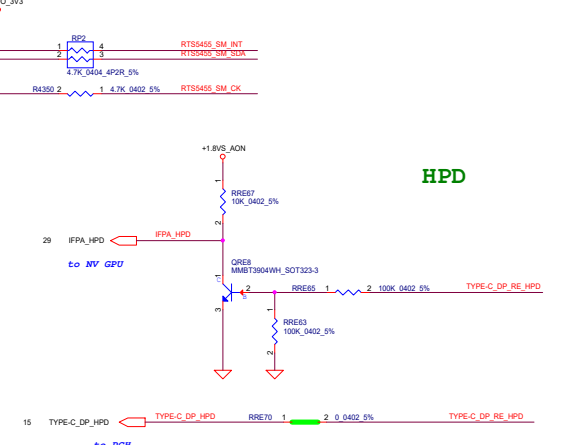
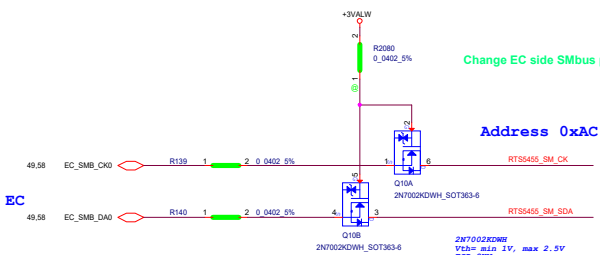
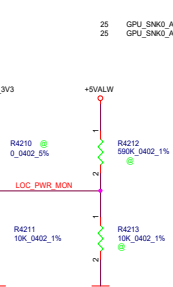
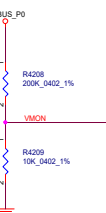
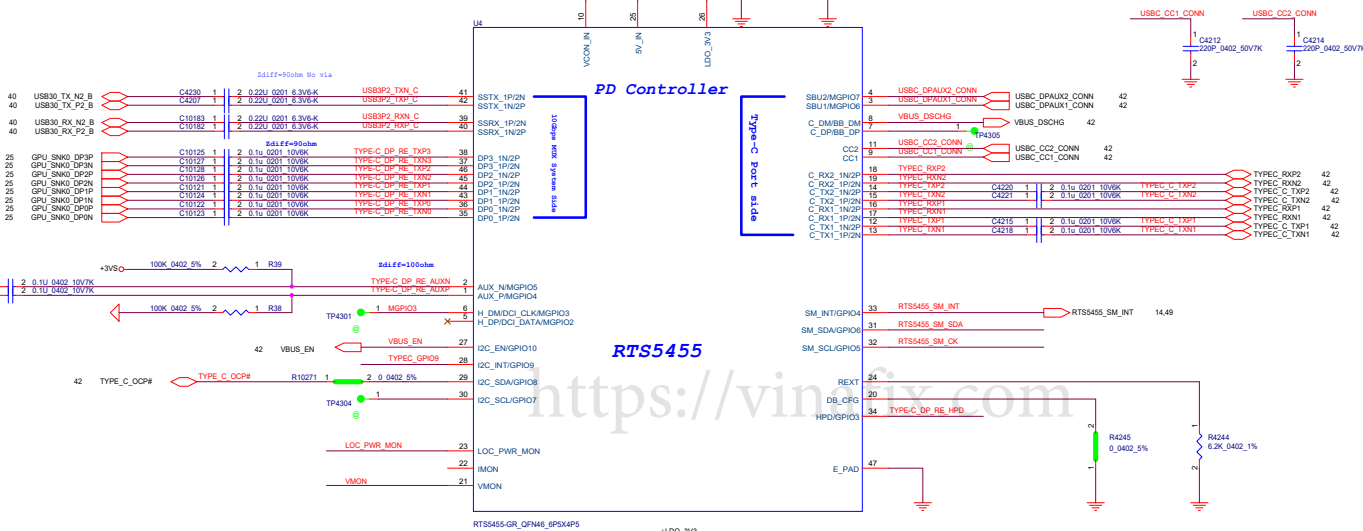
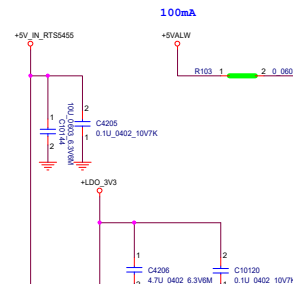
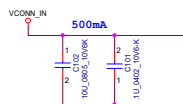
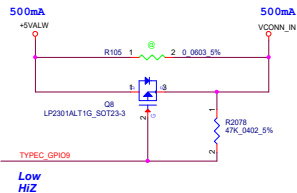


LCD POWER CIRCUIT

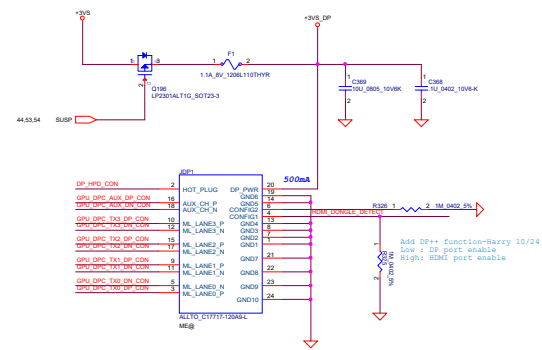
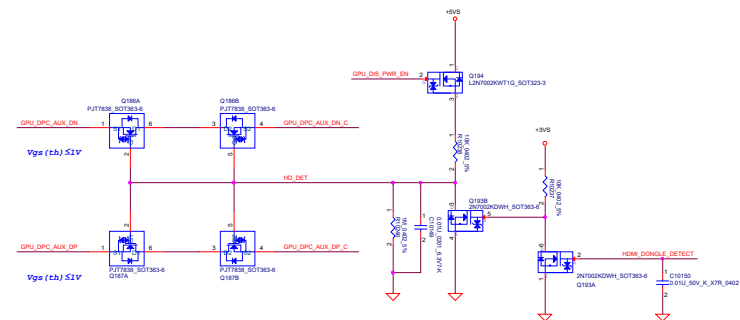
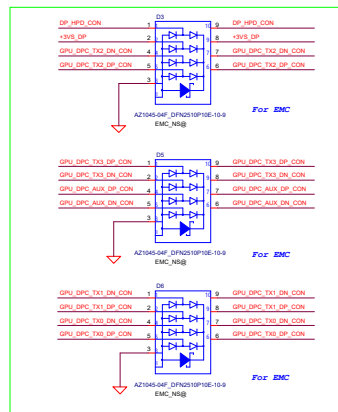




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Issued Date	2018/08/02	Deciphered Date	2018/08/02	Size	Document Number
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			Date	Friday, March 22, 2019	Sheet 39 of 77

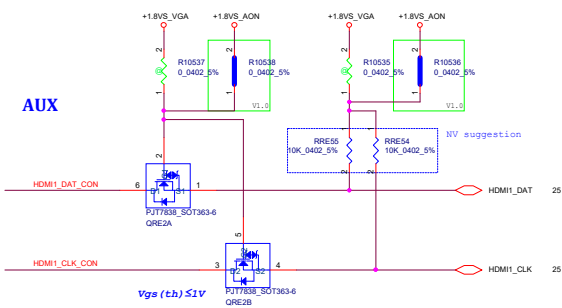
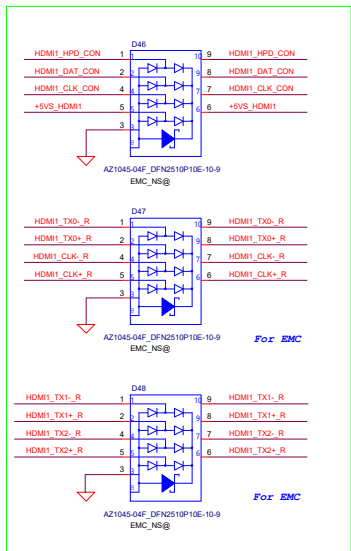
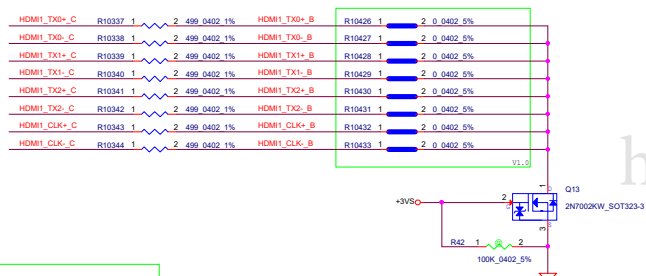
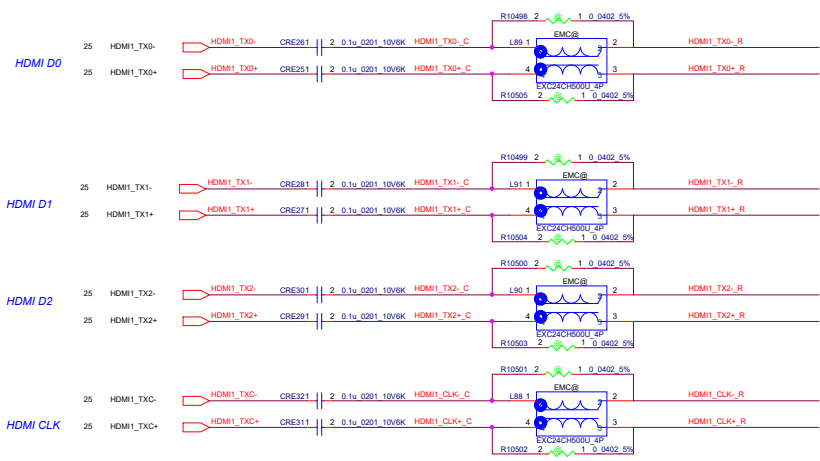
Slave Addr	Ra 1%	Rb 1%
addr0	NC	10K
addr1	54.9K	12.1K
addr2	27.4K	15.8K
addr3	18.2K	22.1K



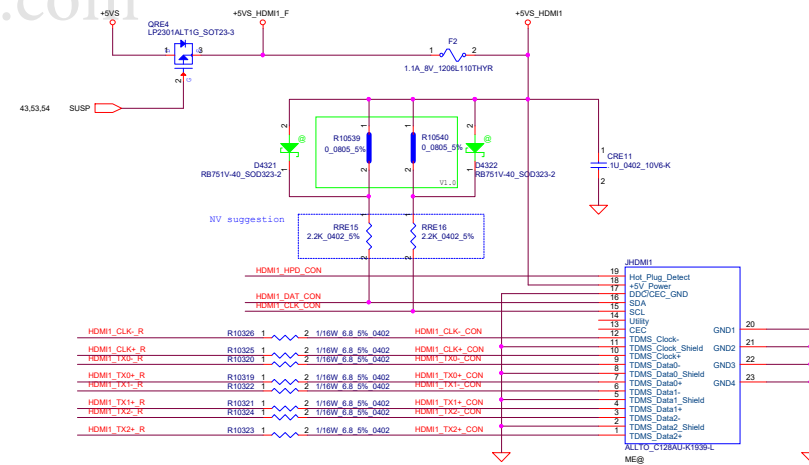
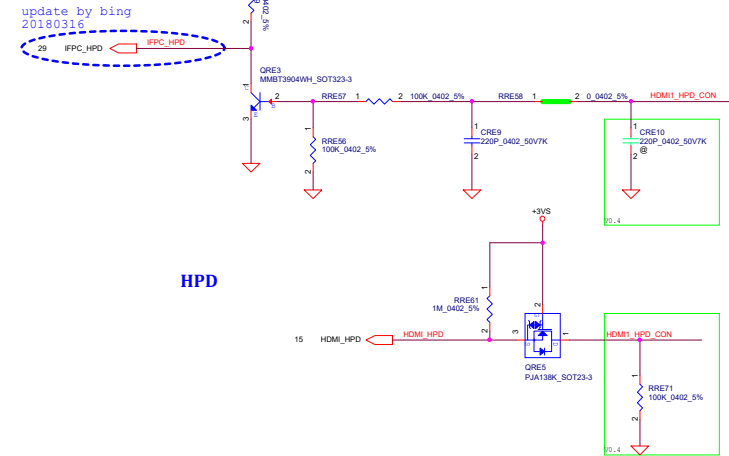
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	USB TYPE-C Controller
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Size	Document Number	Y540		Rev
Contin		Friday, March 23, 2018		2.0
Date		Sheet	41	of 77



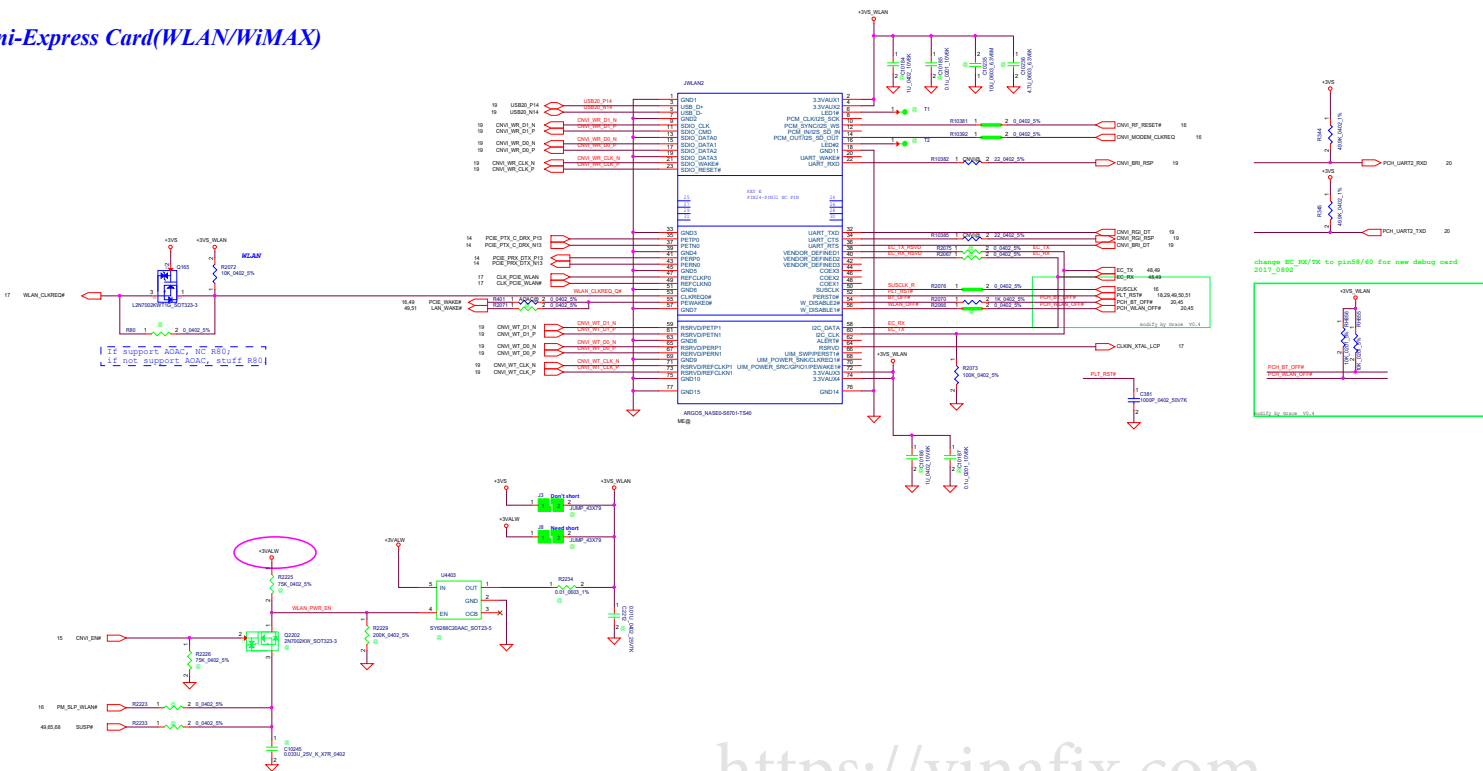
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2018/08/02	Declassified Date	2018/08/02	DP	
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Doc # Y540 Date FRIED, APR 24, 2019					Rev 0 11



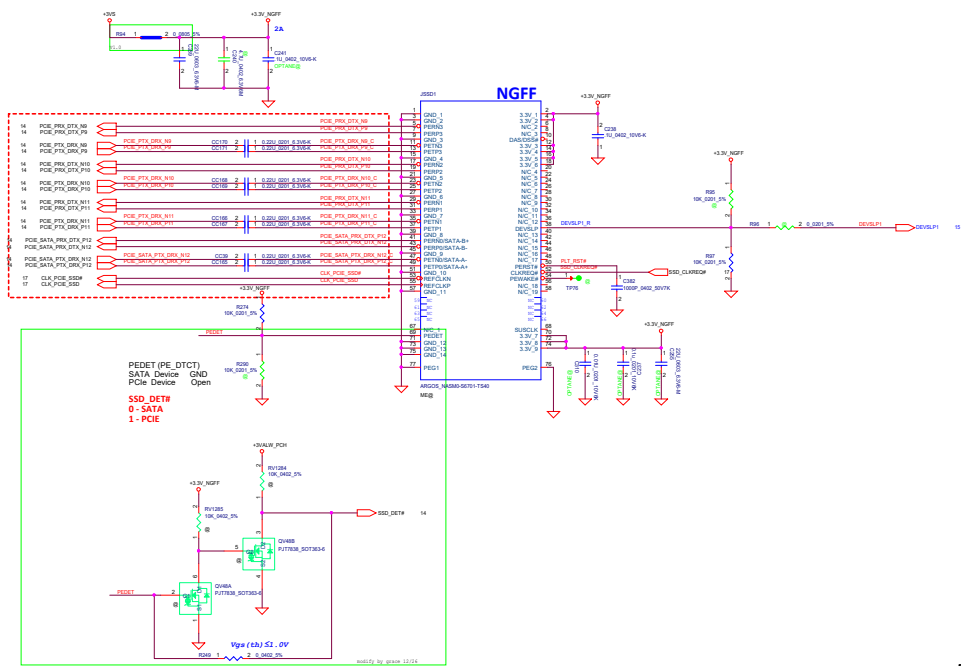
Security Classification	LC Future Center Secret Data		Title	HDMI_CONN	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Size	Document Number
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Date:	Friday, March 22, 2019	Sheet	44	of	77



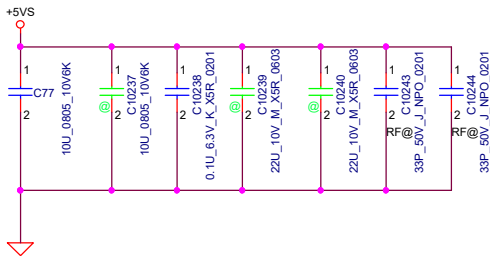
Mini-Express Card(WLAN/WiMAX)



M.2 SSD(SATA/PCIE)



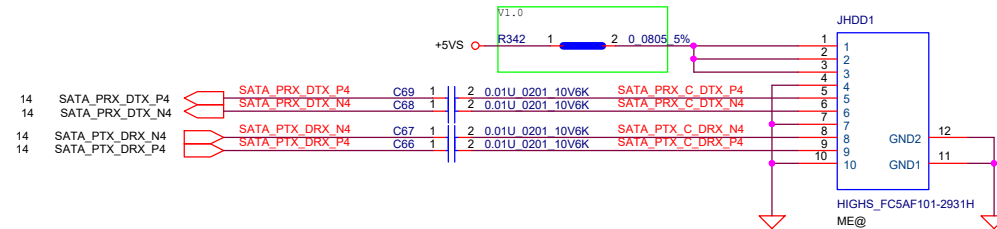
Security Classification	LC Future Center Secret Data		Title	NGFF WLAN
Issued Date	2018/03/02	Declassified Date	2018/03/02	
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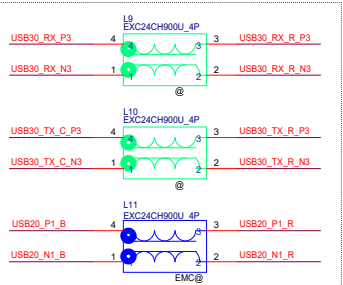
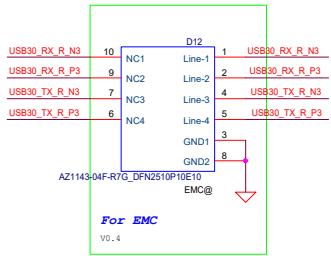
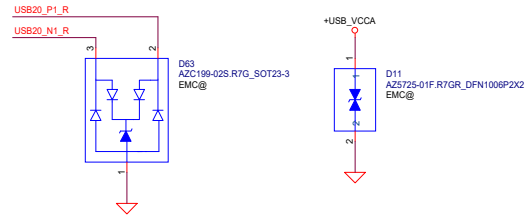
Vinafix.com

<https://vinafix.com>

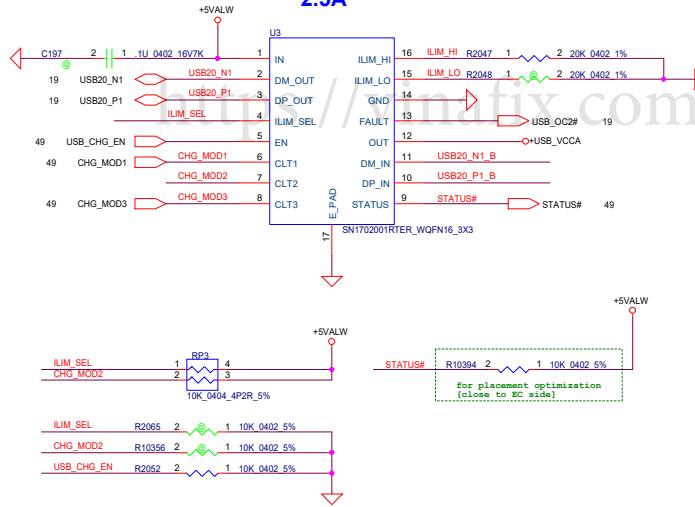
SATA HDD Conn.



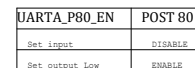
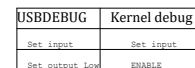
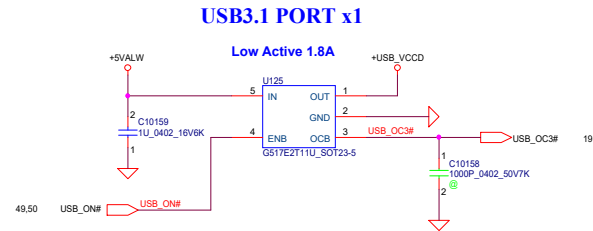
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	HDD/XBOX CONN	
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				Date:	Friday, March 22, 2019
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				Rev	2.0



USB charger 2.5A



CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active



2 Debug_1

3 Debug_2

4 Debug_3

5 Debug_4

11 Debug_5

USBDBUG

R531

0_0402_5%

USB_UART_SEL

U129

1D+

1D-

2D+

2D-

GND1

GND2

OE#

NCY3958Y

10 VCC

9 USB_UART_SEL

8 USBP2+_S

7 USBP2-_S

6

R10450

Debug_1 0_0402_5%

Debug_2 0_0402_5%

Debug_3 0_0402_5%

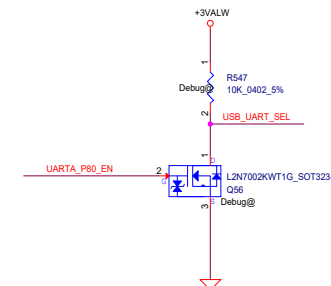
Debug_4 0_0402_5%


Debug_5 0_0402_5%

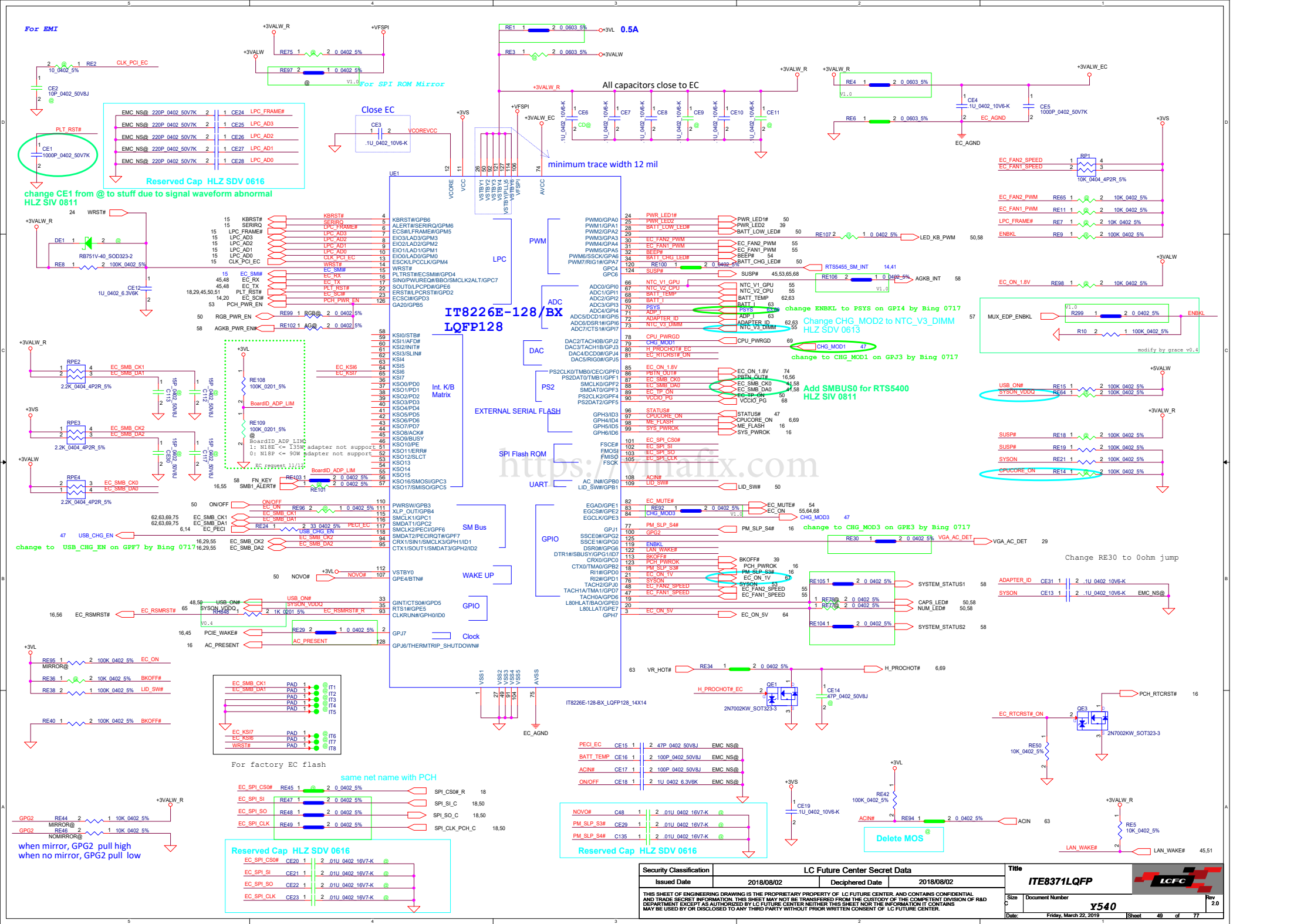
Debug_6 0_0402_5%


3V3ALW

NCY3958Y_DFN10_3X3

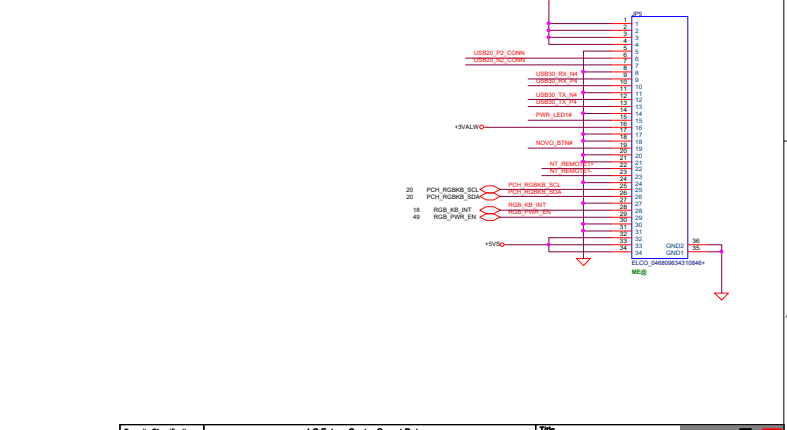
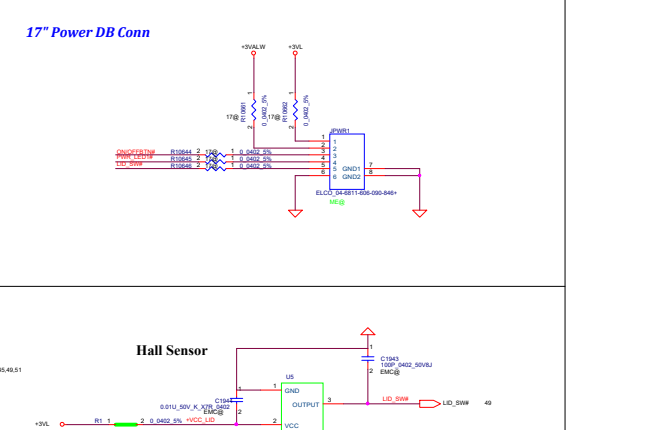
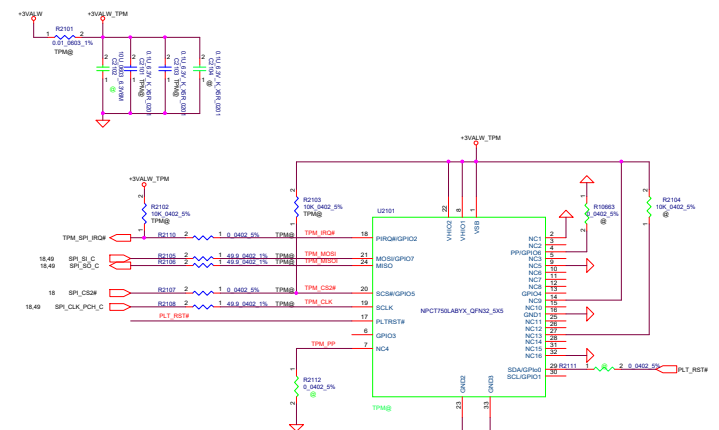
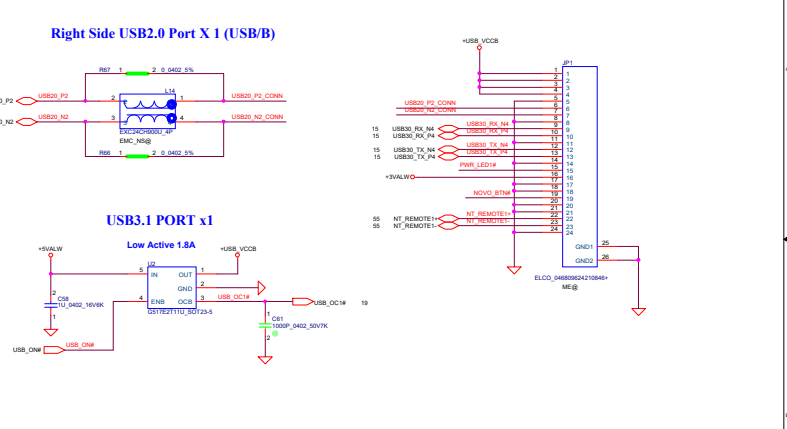
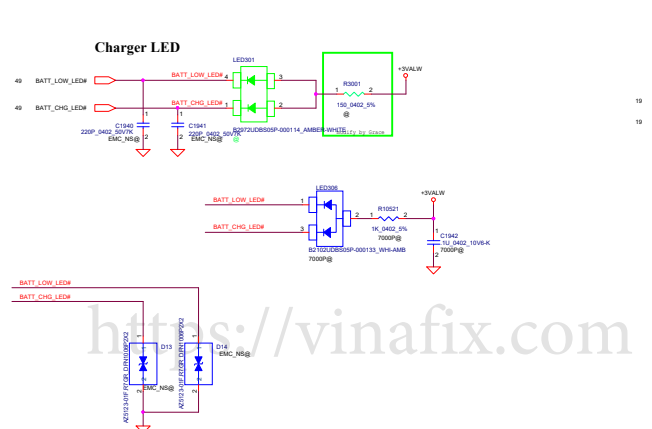
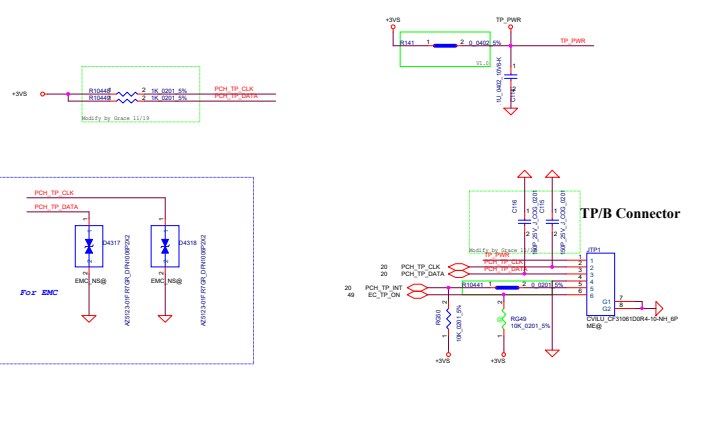
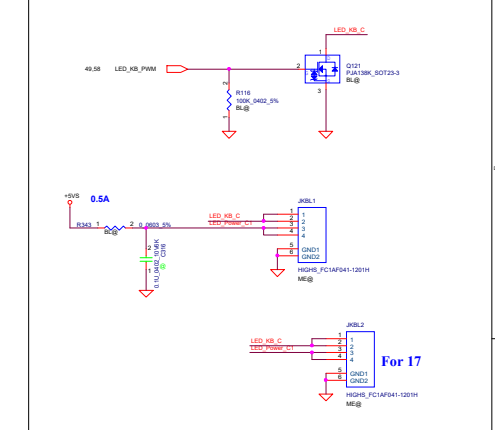
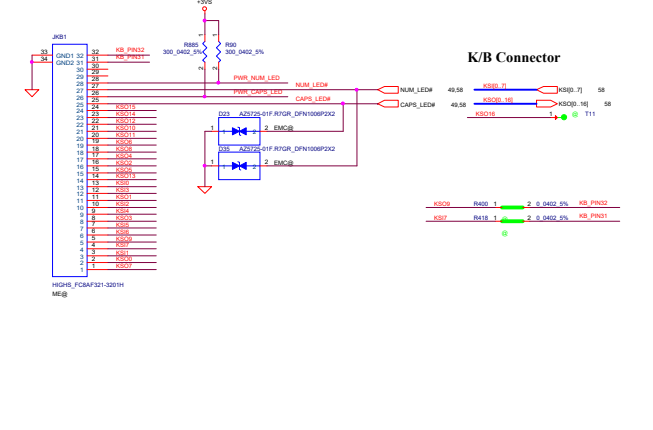
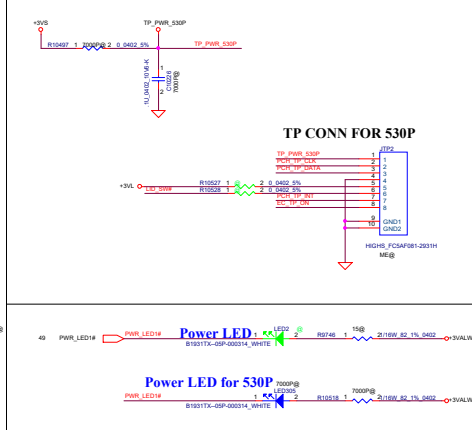
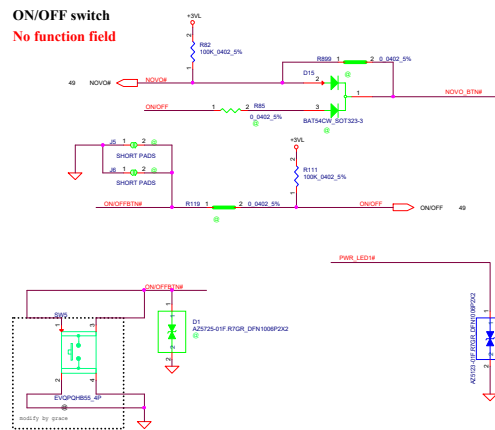


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Date:				Friday, March 22, 2019				Sheet		48 of 77			



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Issued Date	2018/08/02	Deciphered Date	2018/08/02	ITE8371LQFP 	
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Date: Friday, March 22, 2019				Sheet	49 of 77

ON/OFF switch
No function field



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Issued Date	20180802	Designed Date	20180802
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Rev	1	Revision Number	Y540
Date	20180802	Rev	1

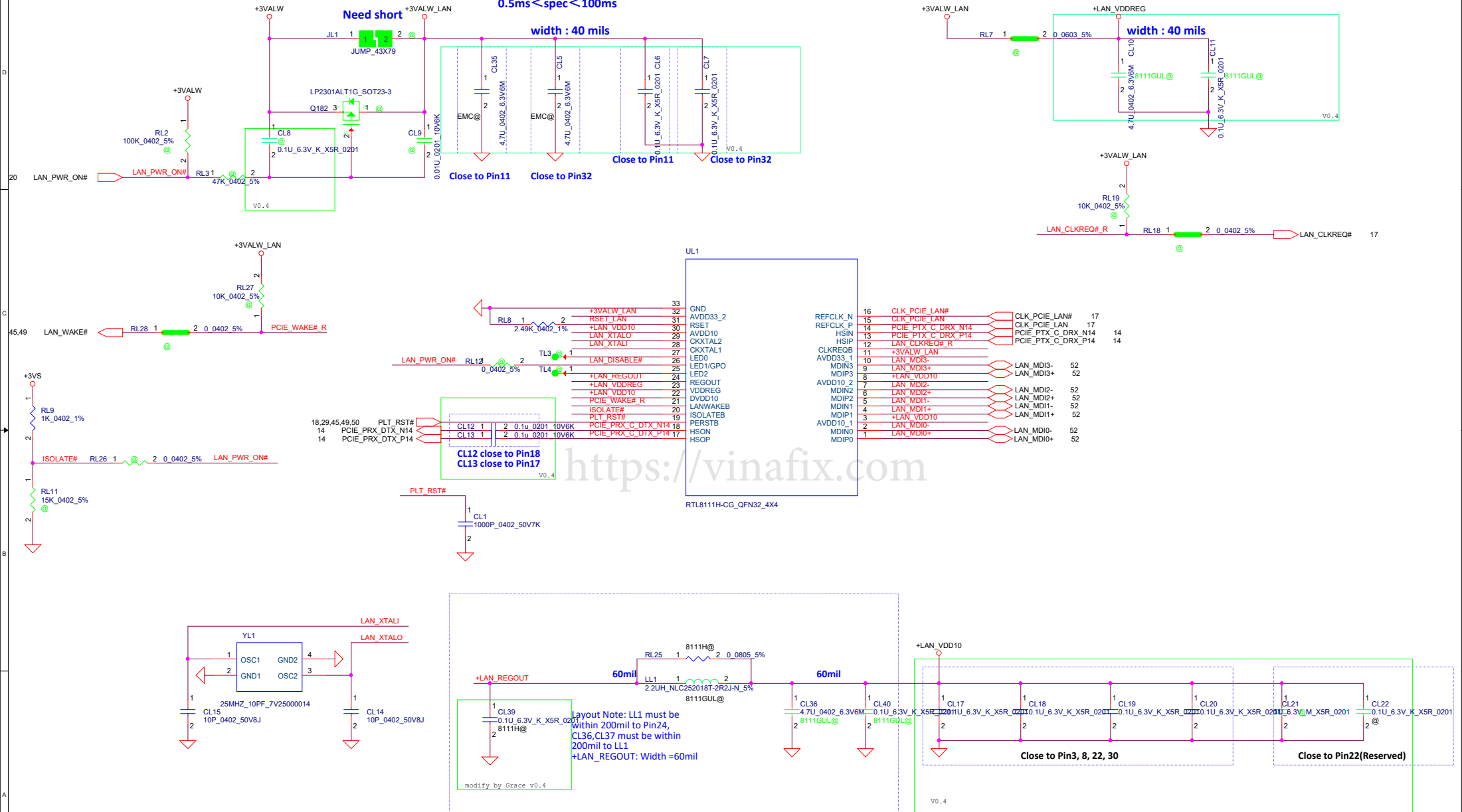
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms < spec < 100ms

Need short

width : 40 mils

width : 40 mils



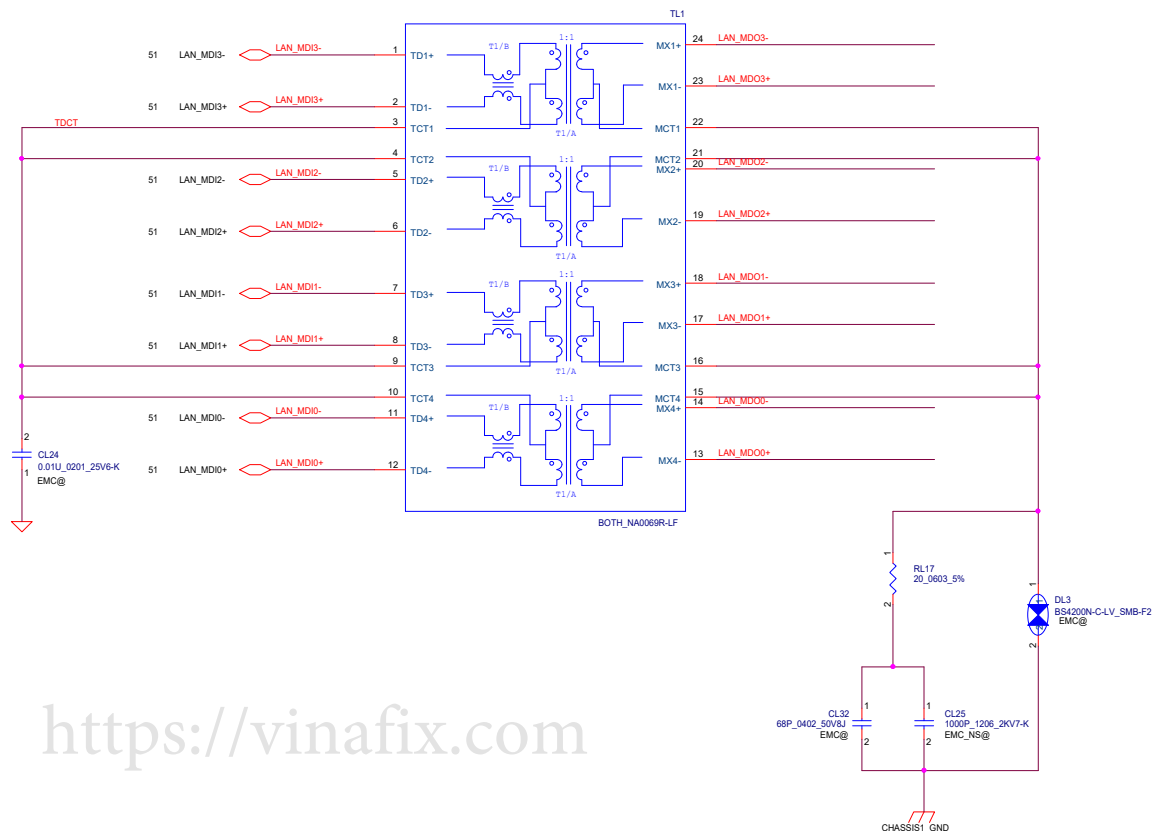
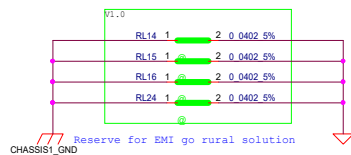
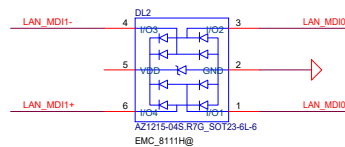
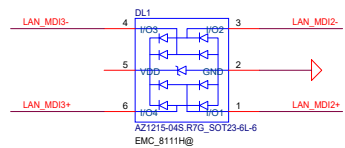
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Issued Date	2018/08/02	Deciphered Date	2018/08/02
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Title		LAN_RTL8111	
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Date	Friday, March 22, 2019	Sheet	51 of 77



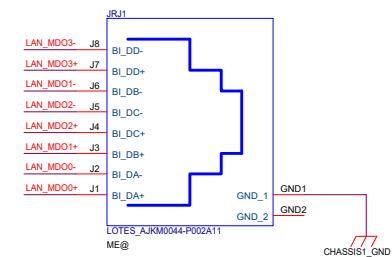
DL1/DL2
1'S PN:SC300005900

Place Close to TL1

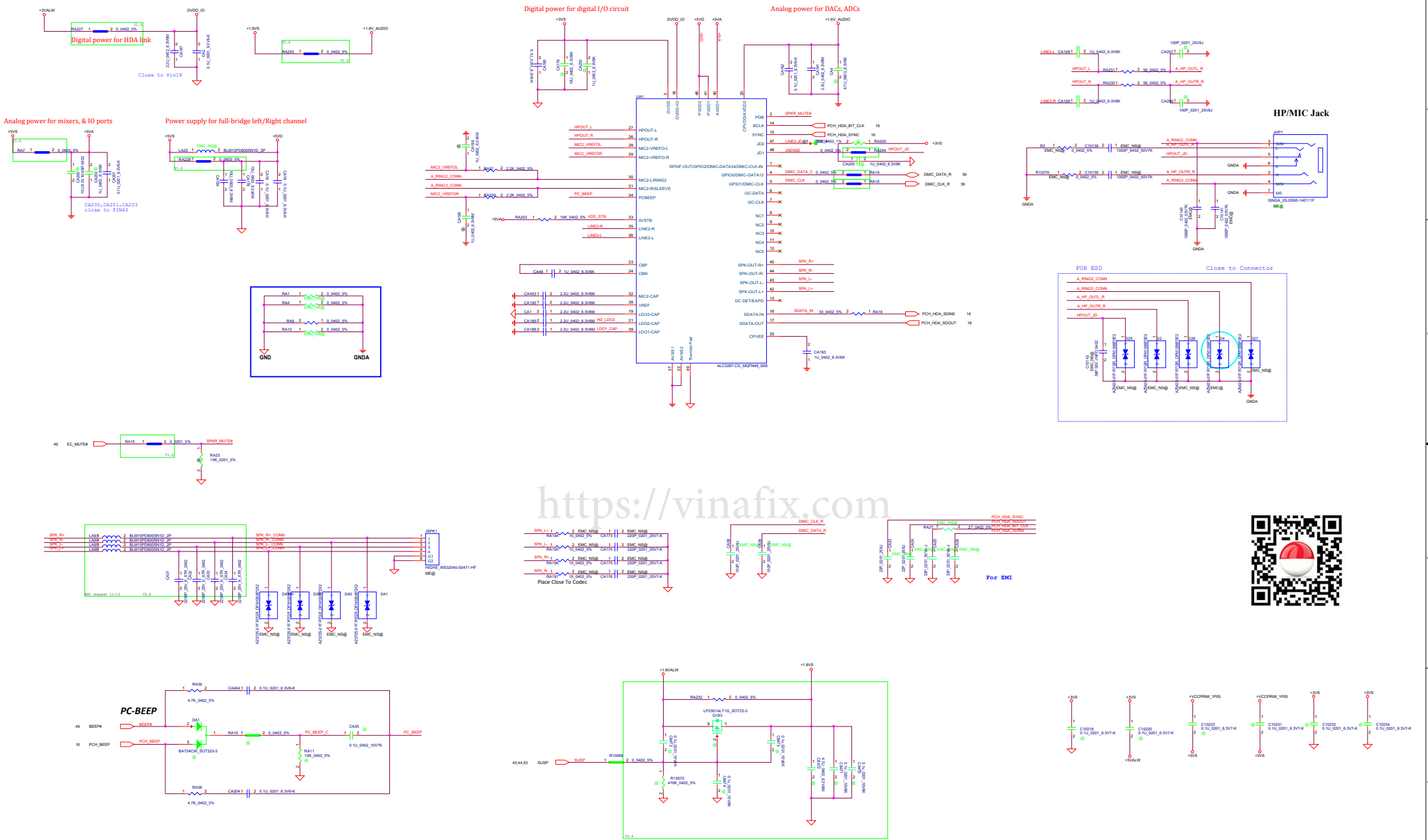


<https://vinafix.com>

Vinafix.com



Security Classification	LC Future Center Secret Data		Title	LAN_Transformer	
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Size	Document Number
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				Date: Friday, March 22, 2019	Sheet 52 of 77

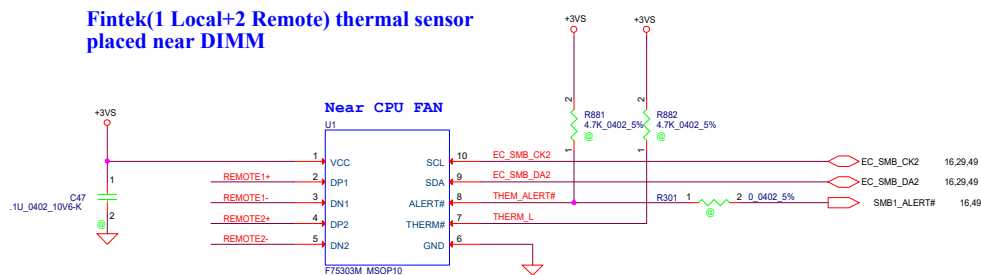


<https://vinafix.com>

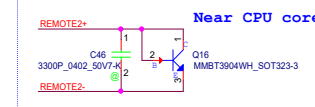
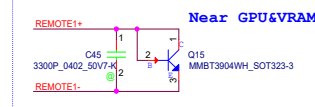


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Rev	D	Revised Number	Y540
Date: 19/08/2018 14:00:00			

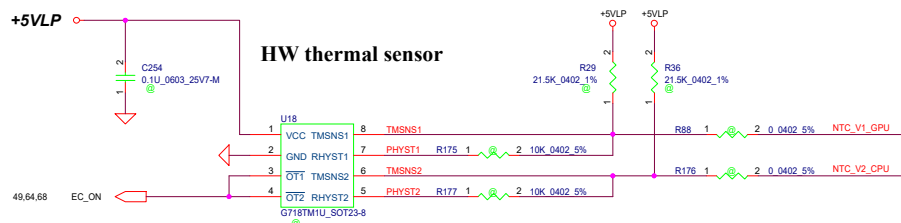
Fintek(1 Local+2 Remote) thermal sensor placed near DIMM



REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

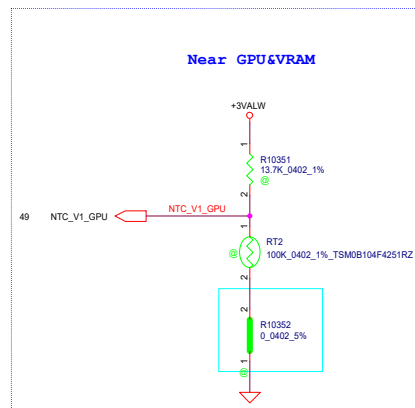


HW thermal sensor

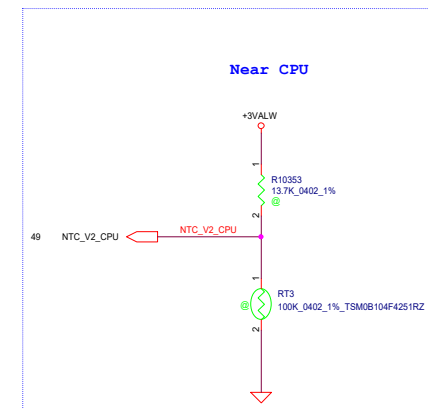


over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

Near GPU&VRAM



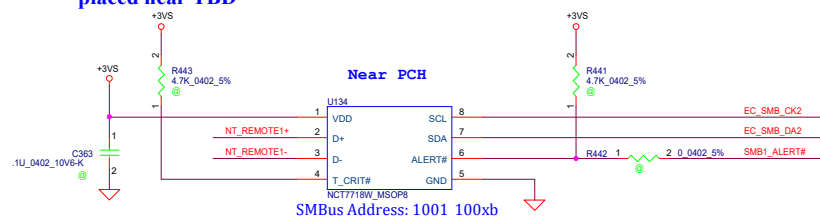
Near CPU



<https://vinafix.com>

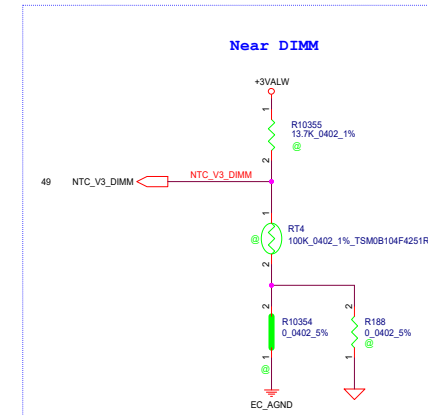
for layout optimized, change the EC_AGND to GND

Nuvoton(1 Local+1 Remote) thermal sensor placed near TBD



Thermal Diode Near GPU FAN(DB)
NT_REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"

Near DIMM



FAN Conn

Address 1001_101xb





TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

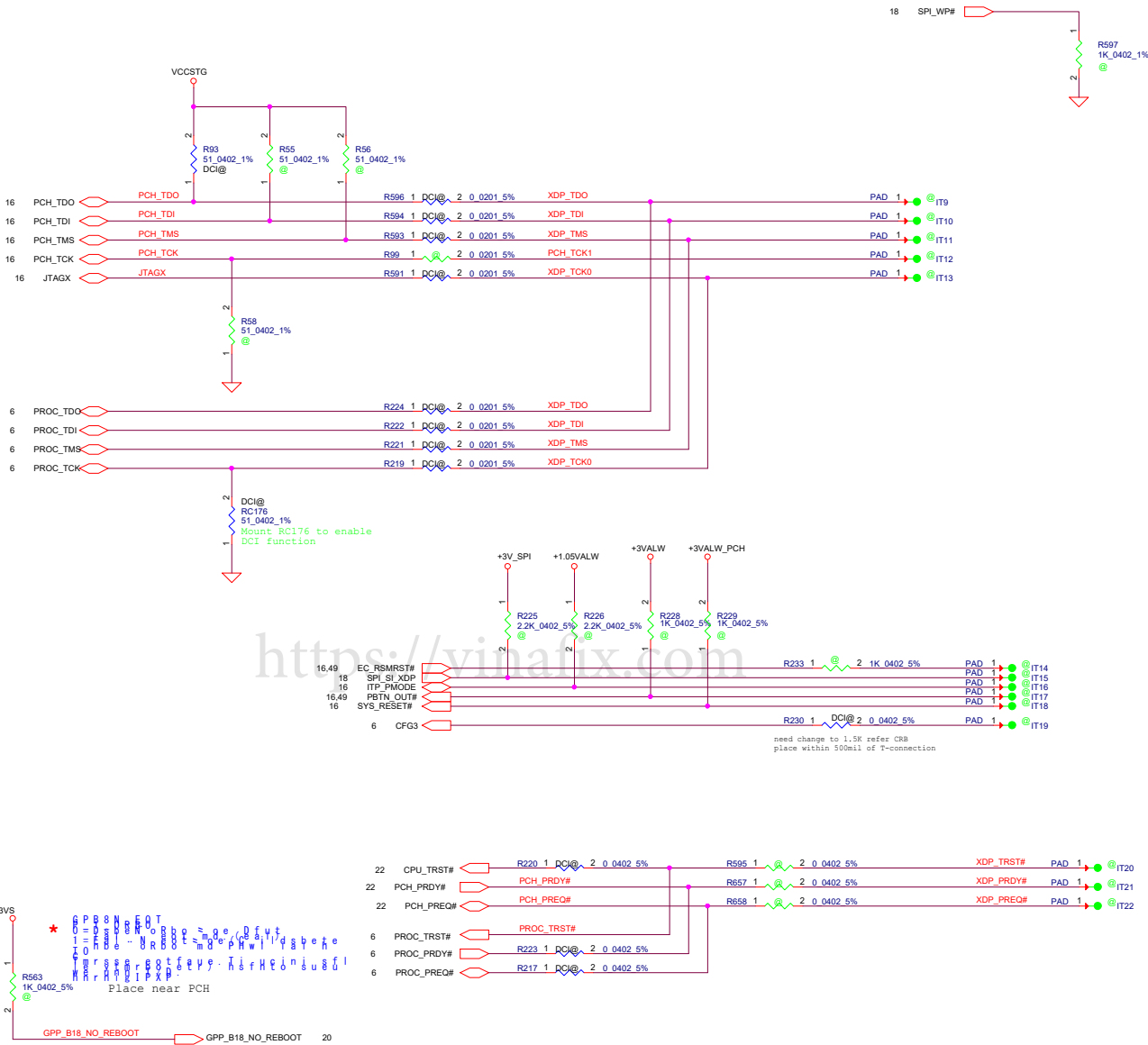
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

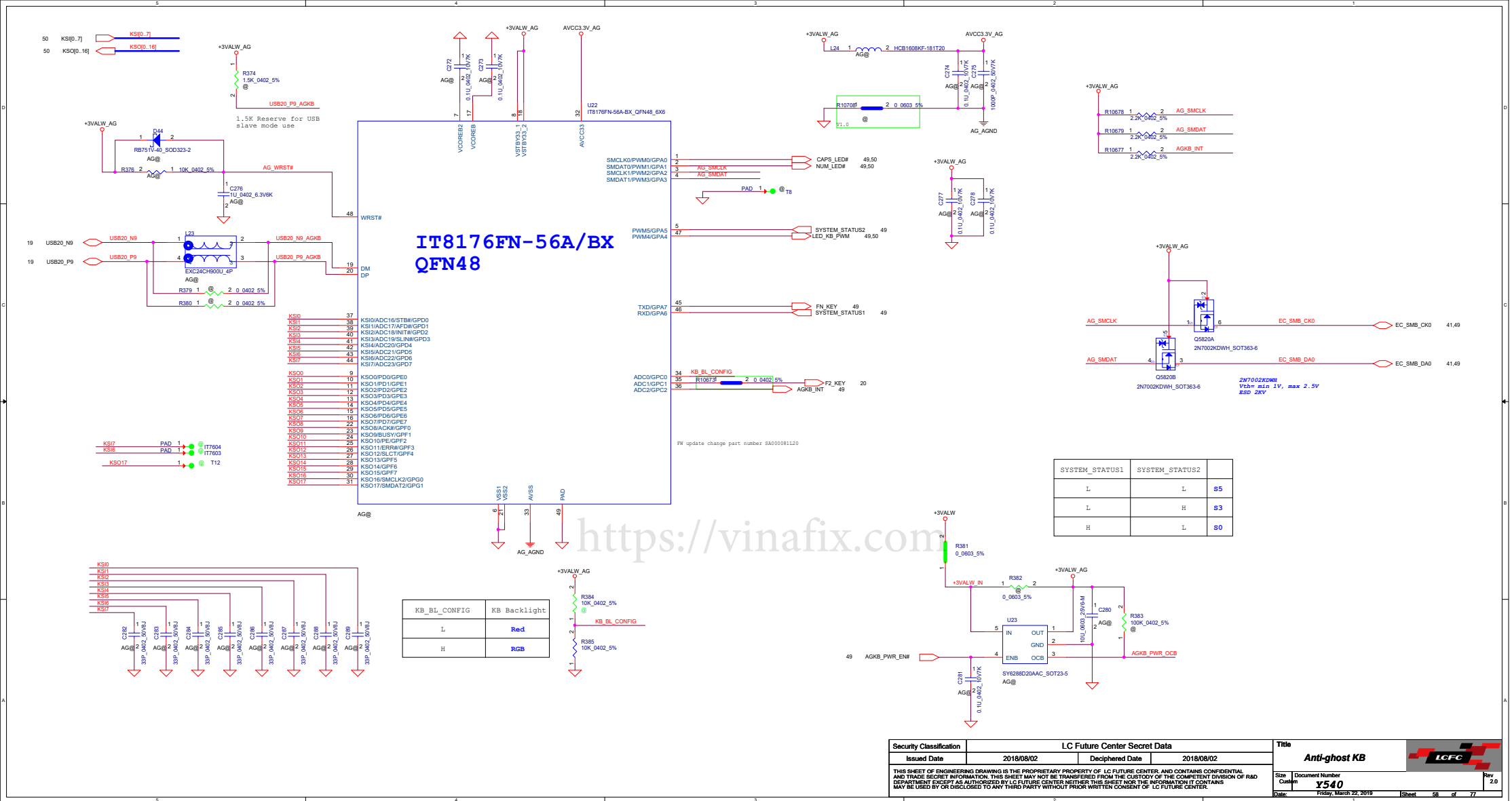
LOGIC

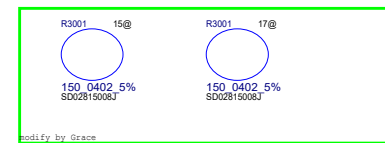
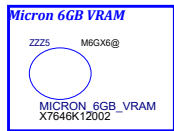
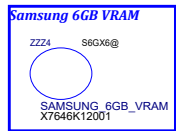
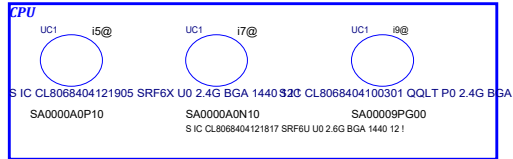
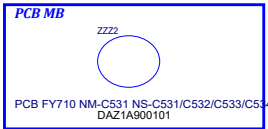
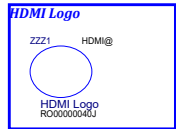
TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

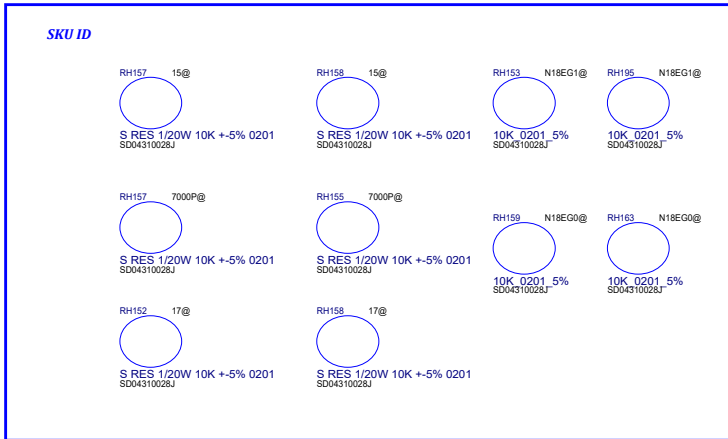
LOGIC

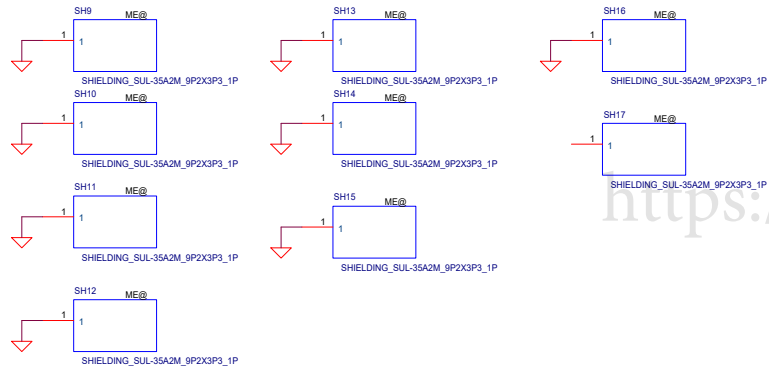
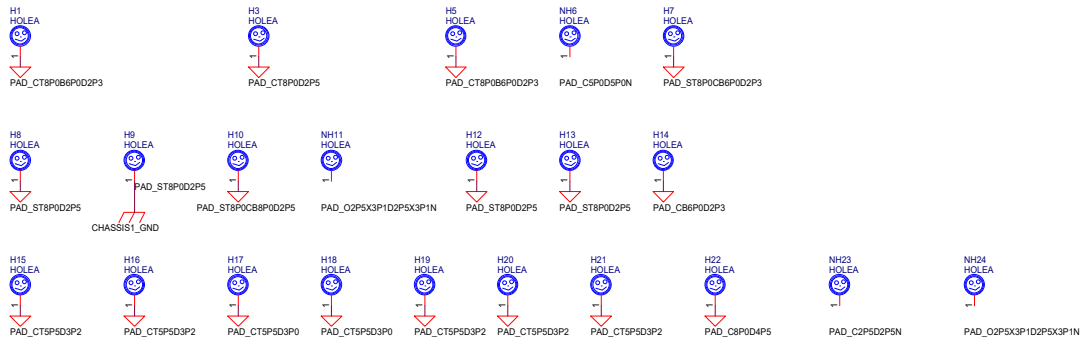




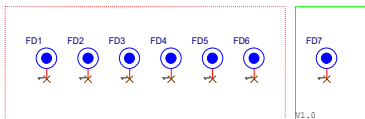


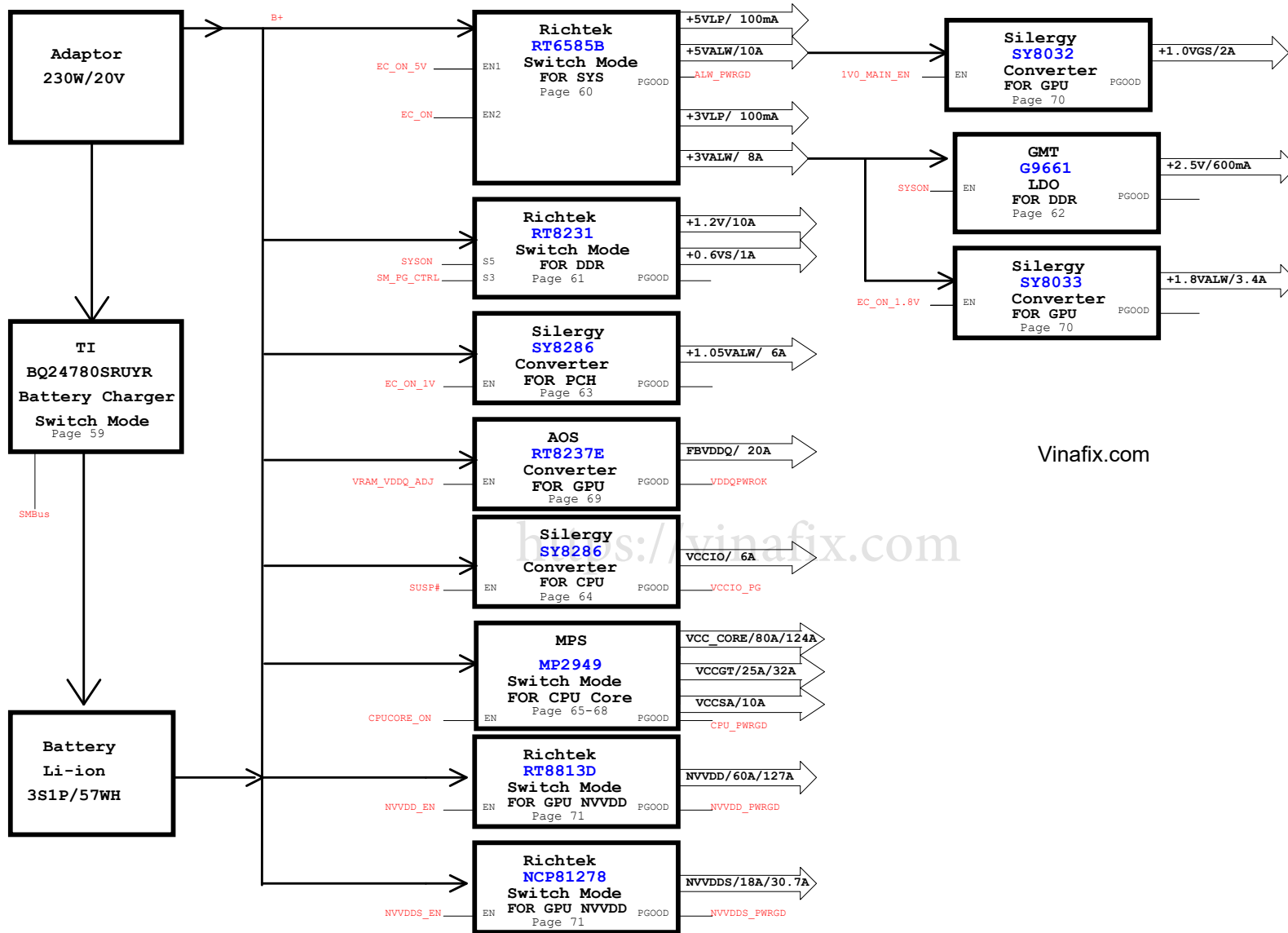
<https://vinafix.com>





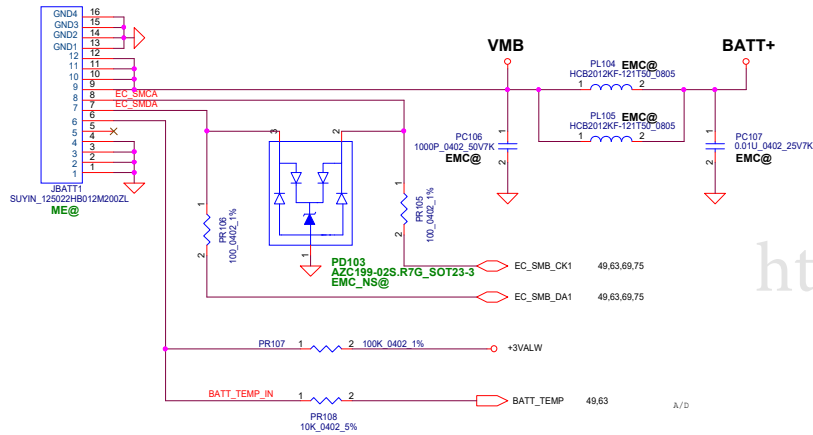
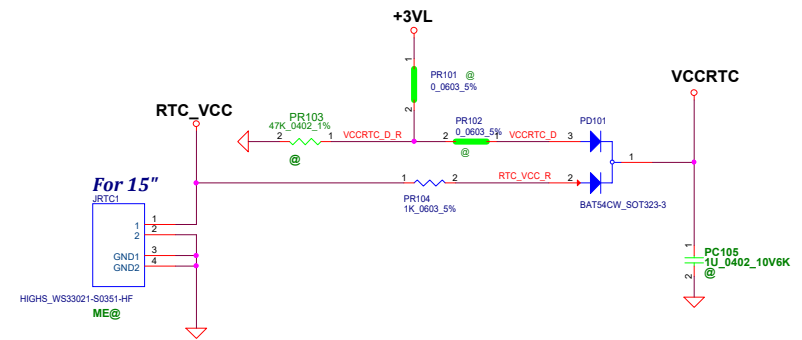
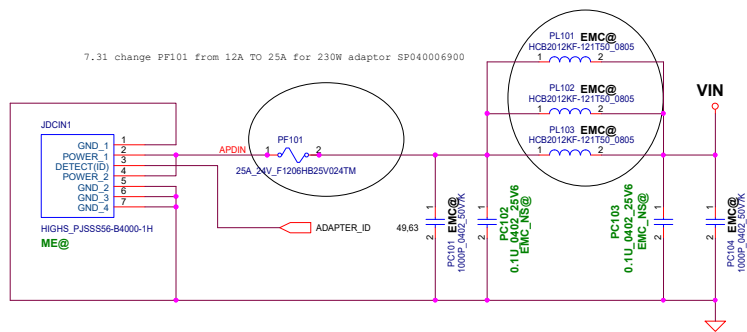
SO-DIMM Shielding



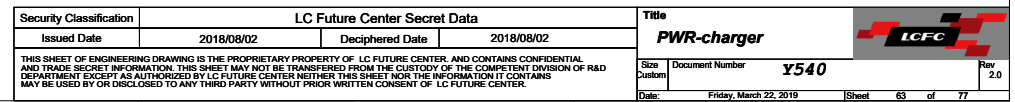


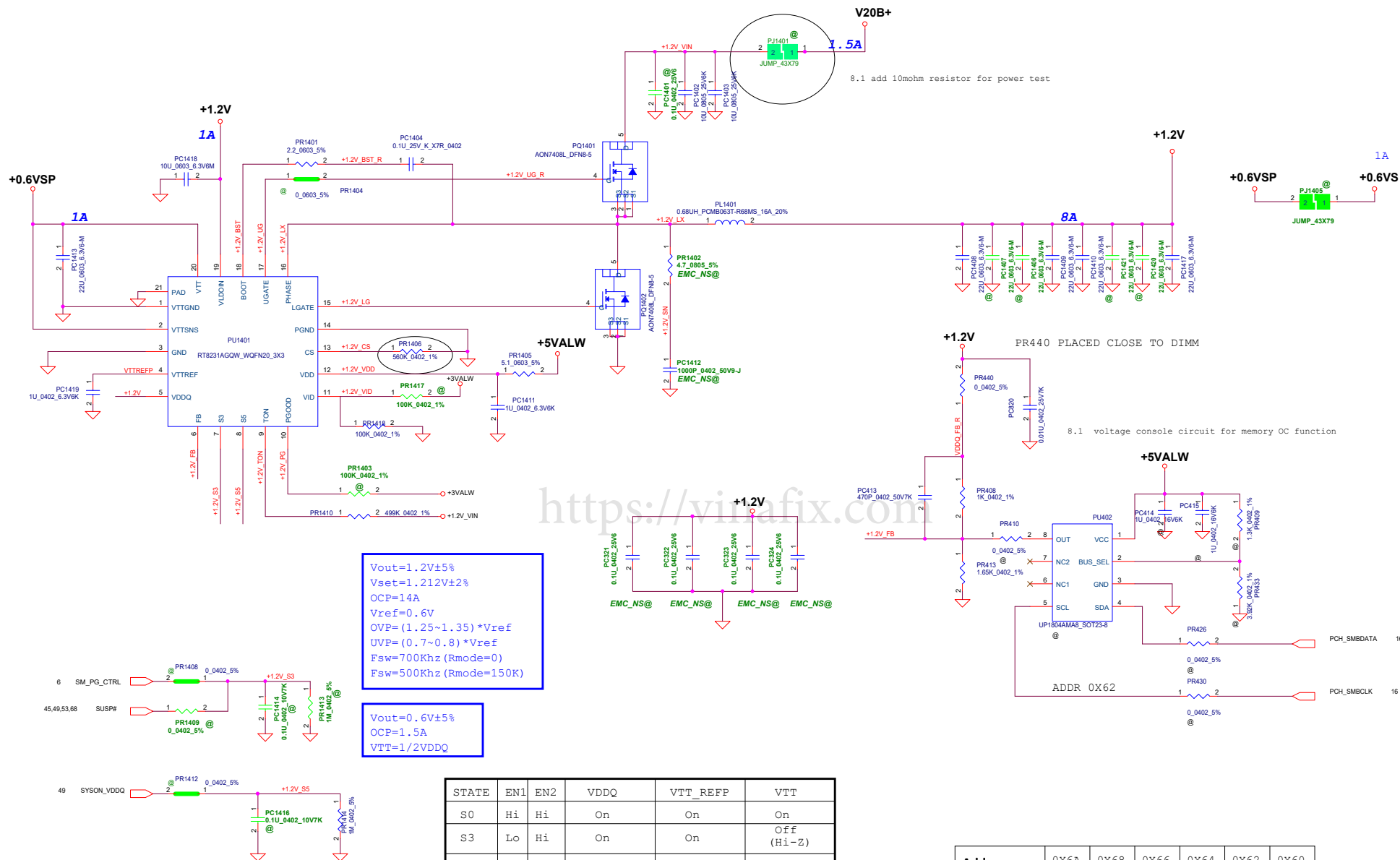
Vinafix.com

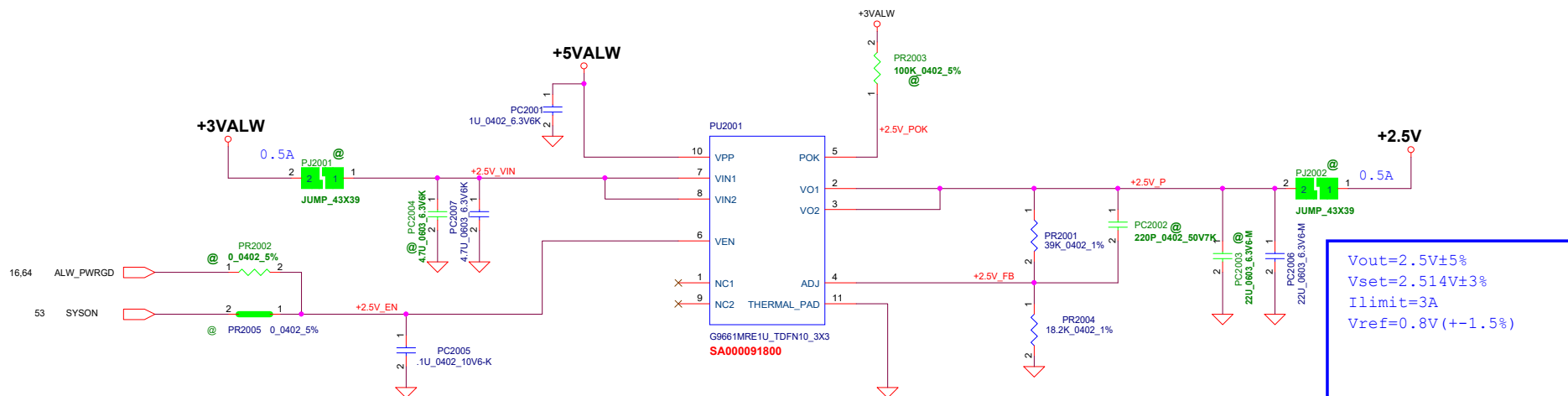




<https://vinafix.com>

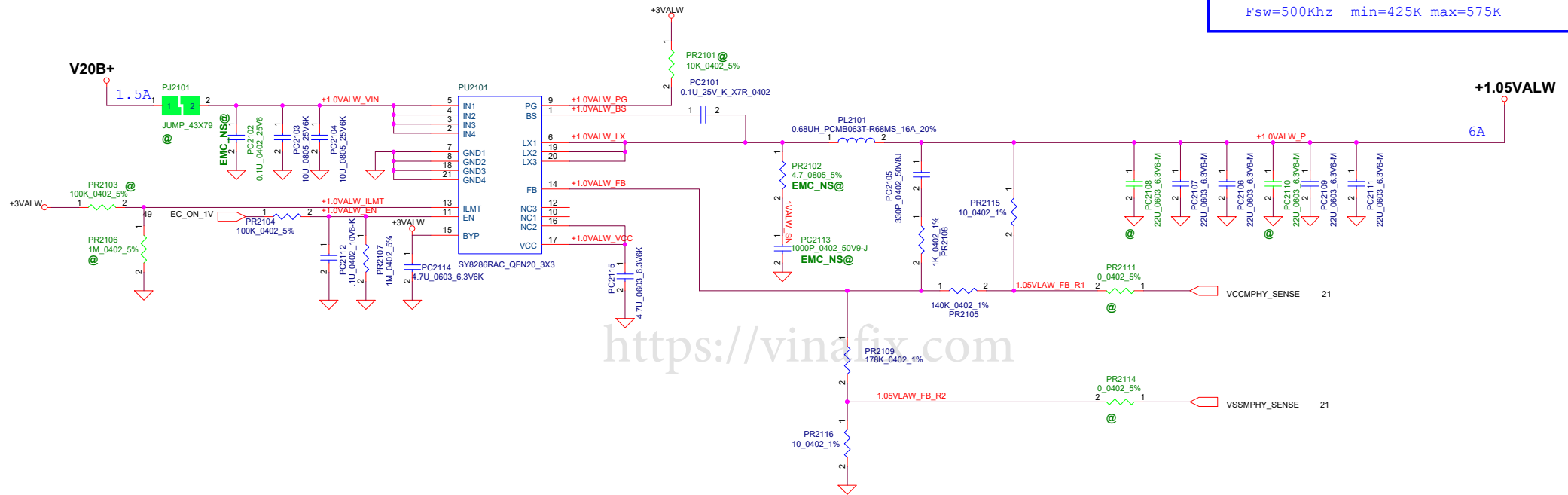






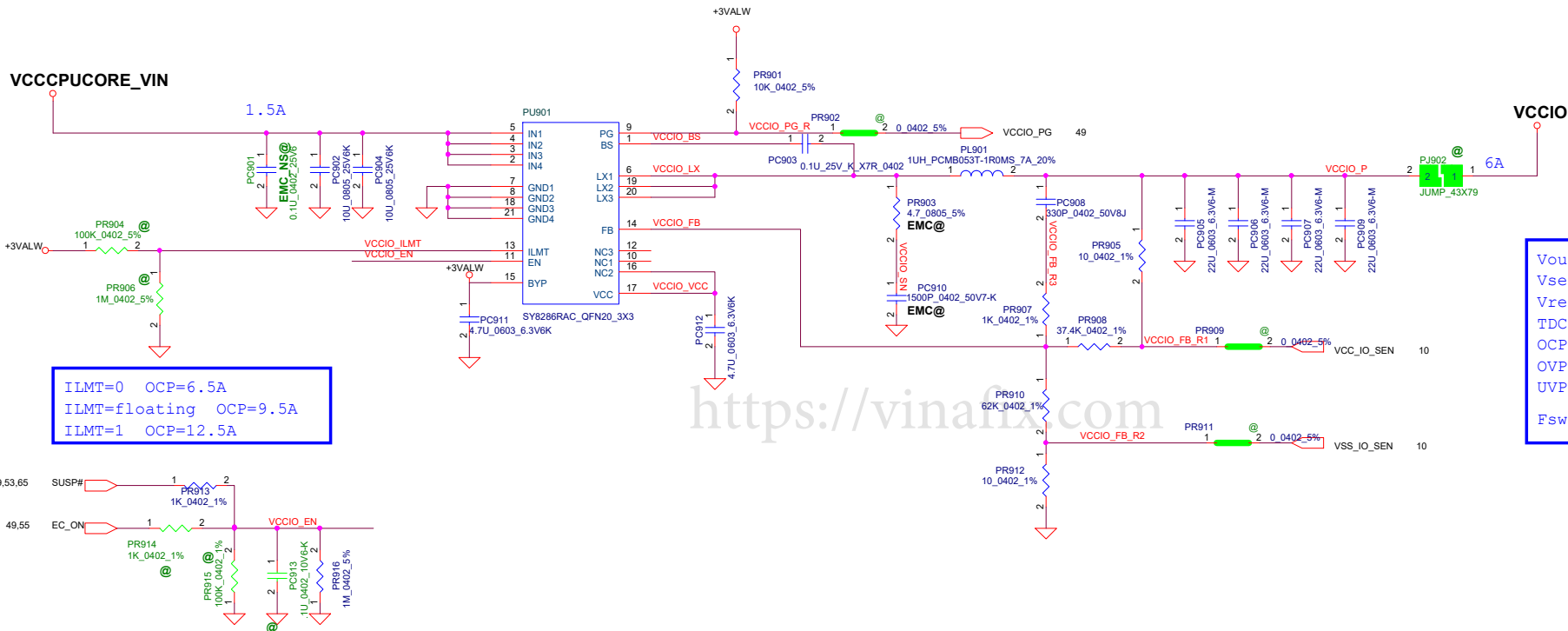
<https://vinafix.com>

$V_{out}=1.05V\pm5\%$
 $V_{set}=1.051V\pm1.81\%$
 $V_{ref}=0.6V(+1\%)$
 $TDC=8A$
 $OCP=12A$
 $OVP=(1.15\sim1.25)*V_{out}$
 $UVP=(0.6\sim0.7)*V_{out}$
 $F_{sw}=500Khz$ min=425K max=575K



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VCCIO 20VB+ change to Core VIN for layout



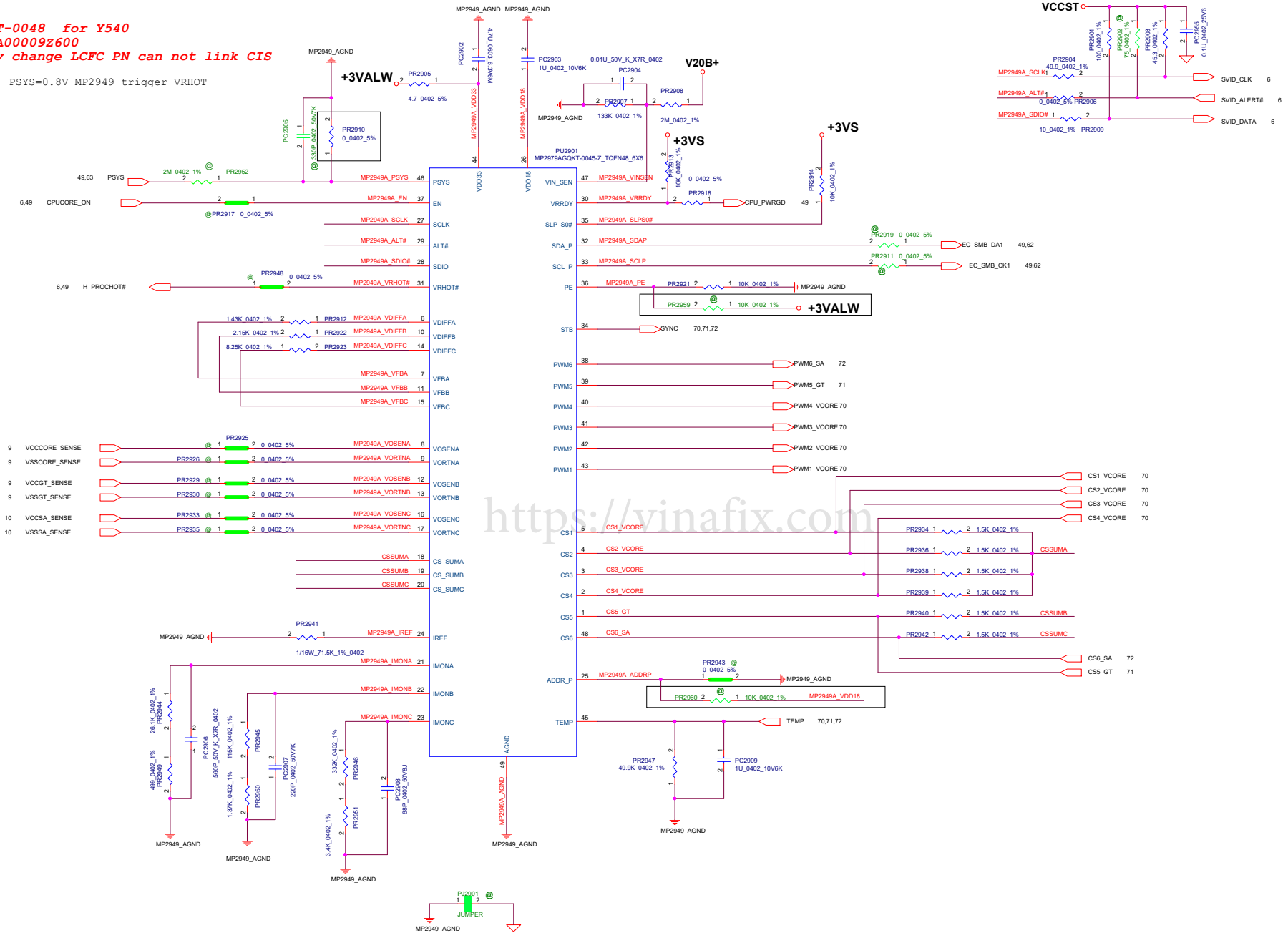
ILMT=0 OCP=6.5A
ILMT=floating OCP=9.5A
ILMT=1 OCP=12.5A


Vout=0.95V±50mV
Vset=0.962V±1.78%
Vref=0.6V
TDC=6A
OCP=9.5A TYP=10.5A MAX 11.5A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K

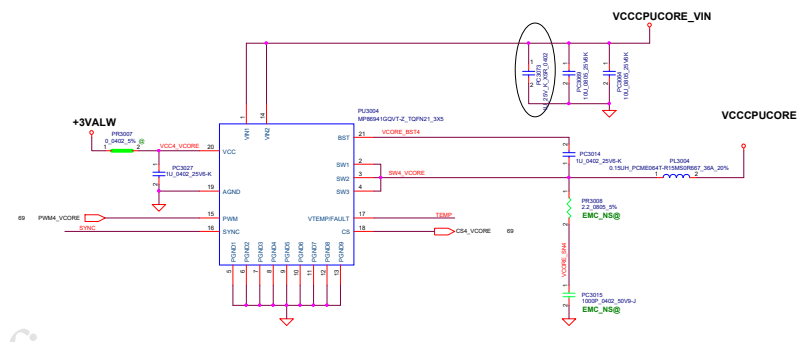
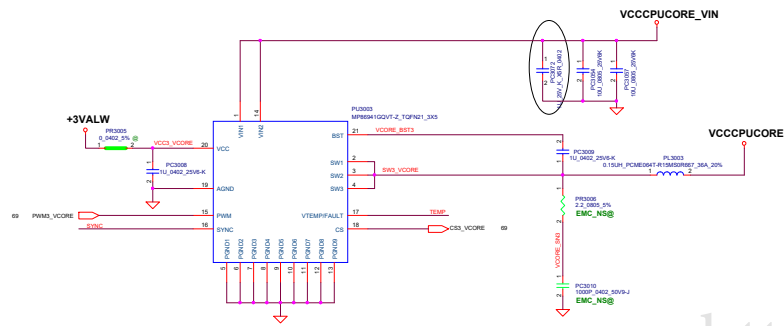
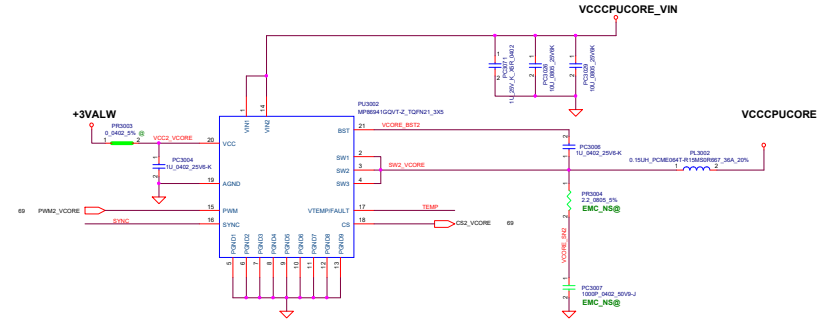
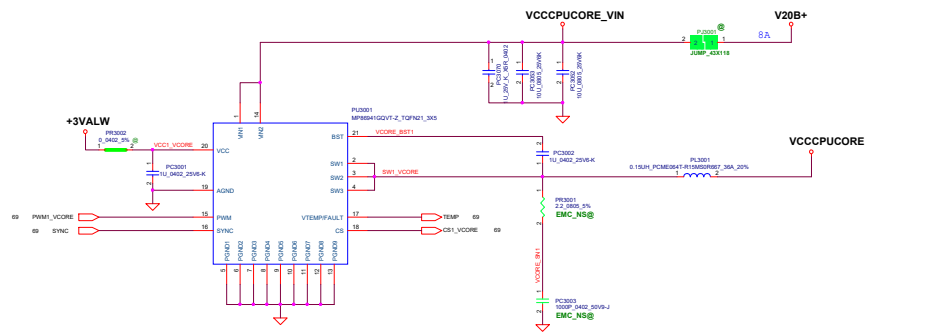
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MP2979AGQKT-0048 for Y540
LCFC PN: SA00009Z600
PU2901 only change LCFC PN can not link CIS

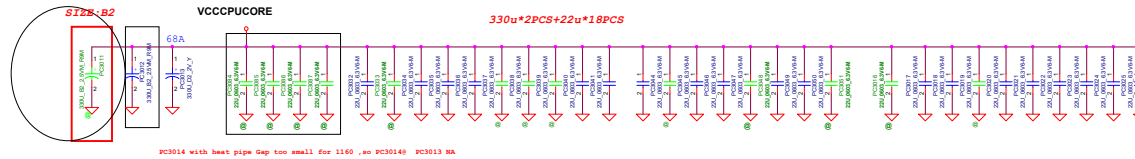
PSYS=0.8V MP2949 trigger VRHOT



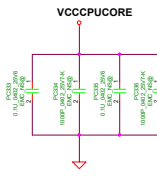
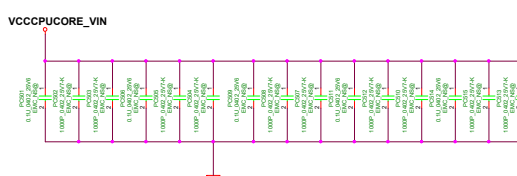
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Issued Date	2016/01/20	Deciphered Date	2016/01/20	PWR-IMPV8_MP2949			
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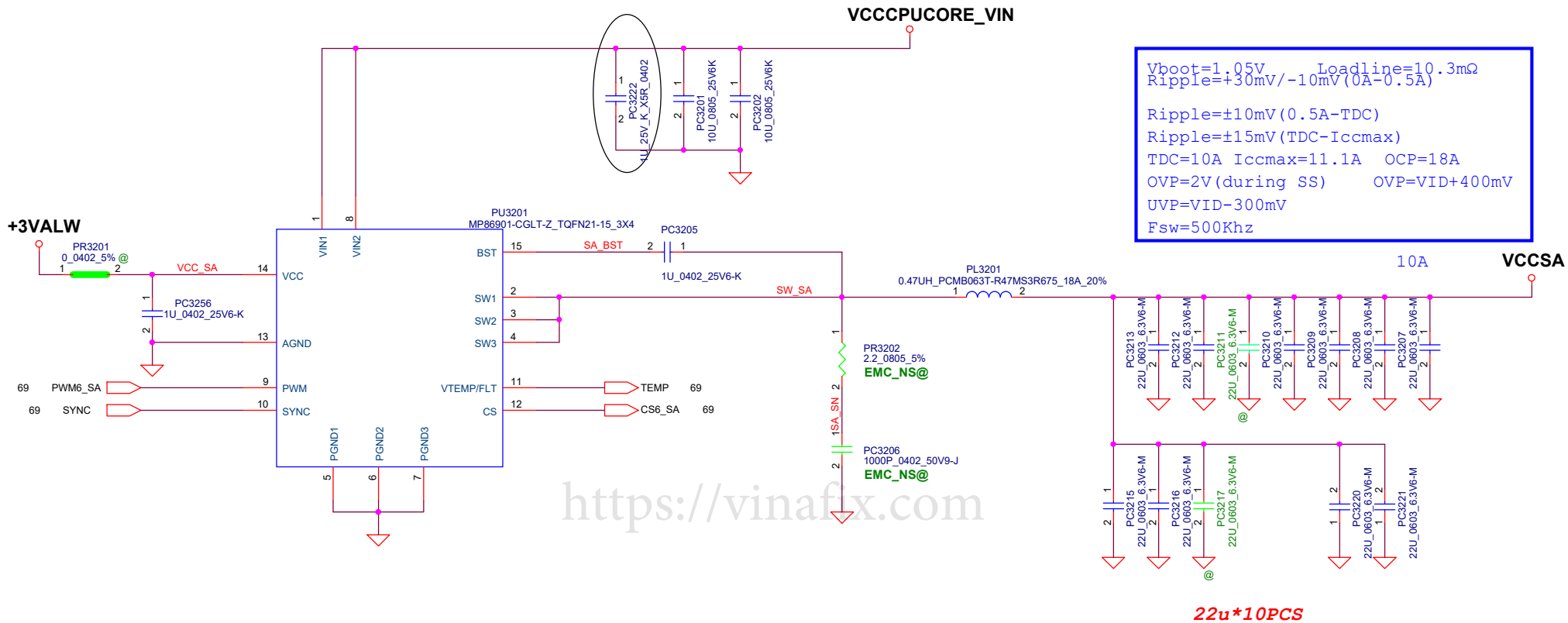
<https://vinafix.com>




Vboot=0V Loadline=1.8mΩ
 Ripple=+30mV/-10mV (0A-0.5A)
 Ripple=10mV (0.5A-TDC)
 Ripple=15mV (TDC-Iccmax)
 TDC=80A (H42 =60A)
 Iccmax=128A (H42 =86)
 OVP=VID+400mV
 OVP=2V (during SS)
 UVP=VID-300mV
 Fsw=500KHz

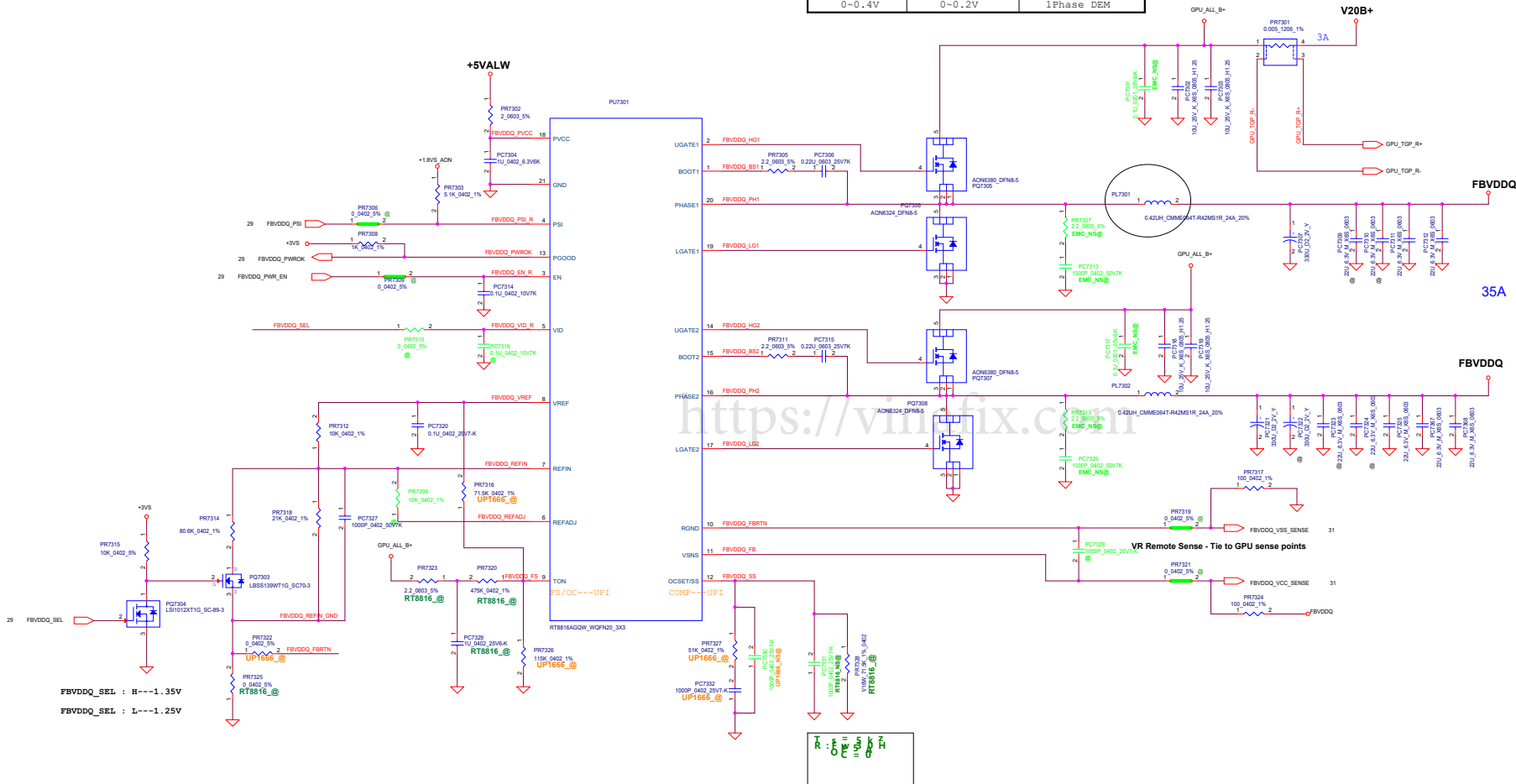


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Rev	Document Number	Y540		Page	
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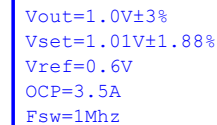
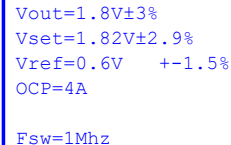



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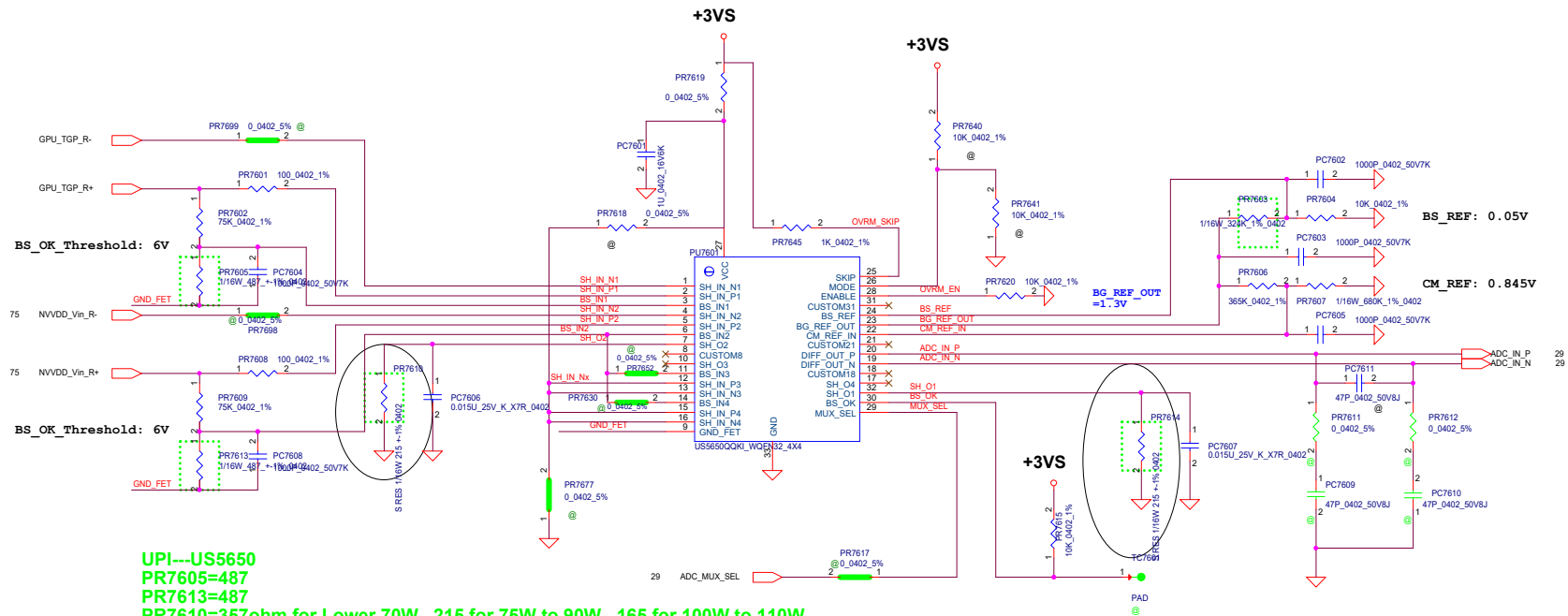
RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM




```
1.8V VIN change to 3.3V
```



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UPI---US5650
 PR7605=487
 PR7613=487
 PR7610=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
 PR7614=357ohm for Lower 70W 215 for 75W to 90W 165 for 100W to 110W
 PR7603=324K
 PR7602=75K
 PR7609=75K
 PC7604=1nF
 PC7608=1nF

ON---NCP45491
 PR7605=649
 PR7613=649
 PR7610=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
 PR7614=475ohm for lower 70W 287 for 75W to 90W 221 for 100W to 110W
 PR7603=243K
 PR7602=75K
 PR7609=75K
 PC7604=1nF
 PC7608=1nF

<https://vinafix.com>

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Security Classification	LC Future Center Secret Data			Title		
Issued Date	2018/08/02	Deciphered Date	2018/08/02	Virtual symbol		
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